SERIPLEX® Control Bus Version 2
Standards Specification
Electrical equipment should be serviced only by qualified electrical maintenance personnel. No responsibility is assumed by Schneider Electric for any consequences arising out of the use of this material.

While effort has been made to ensure accuracy of information and proper operation of the circuits described in this manual, the SERIPLEX Technology Organization makes no warranty regarding the information contained in this manual, and assumes no liability for any injury, loss, or damage that may result directly or indirectly from the use of information contained within this manual.

For more information regarding the use of SERiPLEX technology or to incorporate SERiPLEX ASICs into your products, contact the SERiPLEX Technology Organization, Inc., (STO) at 1-800-SPLXINC (1-800-775-9462).
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Reference Documents</td>
<td>5</td>
</tr>
<tr>
<td>1.2</td>
<td>Technical Philosophy</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>SYSTEM ELEMENTS</td>
<td>7</td>
</tr>
<tr>
<td>3.1</td>
<td>Peer-to-Peer Mode Data Transmission</td>
<td>8</td>
</tr>
<tr>
<td>3.2</td>
<td>Master/Slave Mode Data Transmission</td>
<td>10</td>
</tr>
<tr>
<td>3.3</td>
<td>General Data Transmission Features</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>BUS PHYSICAL CHARACTERISTICS</td>
<td>15</td>
</tr>
<tr>
<td>4.1</td>
<td>Bus Power</td>
<td>15</td>
</tr>
<tr>
<td>4.2</td>
<td>Data Line Characteristics</td>
<td>18</td>
</tr>
<tr>
<td>4.3</td>
<td>Clock Line Characteristics</td>
<td>19</td>
</tr>
<tr>
<td>4.4</td>
<td>Bus Topology</td>
<td>21</td>
</tr>
<tr>
<td>4.5</td>
<td>Signal Timing</td>
<td>23</td>
</tr>
<tr>
<td>4.6</td>
<td>Environmental Requirements</td>
<td>25</td>
</tr>
<tr>
<td>5</td>
<td>DATA DEFINITIONS</td>
<td>25</td>
</tr>
<tr>
<td>5.1</td>
<td>Special Signal Definitions</td>
<td>25</td>
</tr>
<tr>
<td>5.2</td>
<td>Signal Addressing Conventions</td>
<td>26</td>
</tr>
<tr>
<td>5.3</td>
<td>Bit Order</td>
<td>27</td>
</tr>
<tr>
<td>5.4</td>
<td>Data Coherence</td>
<td>27</td>
</tr>
<tr>
<td>6</td>
<td>OPERATIONAL CHARACTERISTICS</td>
<td>27</td>
</tr>
<tr>
<td>6.1</td>
<td>Bus Initialization</td>
<td>27</td>
</tr>
<tr>
<td>6.2</td>
<td>Device Initialization</td>
<td>28</td>
</tr>
<tr>
<td>6.3</td>
<td>Normal Bus Operation</td>
<td>28</td>
</tr>
<tr>
<td>6.4</td>
<td>Bus Fault Detection</td>
<td>29</td>
</tr>
<tr>
<td>6.5</td>
<td>Clock-Loss Detection and Response</td>
<td>29</td>
</tr>
<tr>
<td>6.6</td>
<td>Data Error Detection Methods</td>
<td>30</td>
</tr>
<tr>
<td>6.7</td>
<td>Faults and Responses</td>
<td>36</td>
</tr>
<tr>
<td>7</td>
<td>DEVICE PROGRAMMING</td>
<td>40</td>
</tr>
<tr>
<td>8</td>
<td>SIGNAL RESPONSE TIME</td>
<td>41</td>
</tr>
<tr>
<td>8.1</td>
<td>Frame Period (tF)</td>
<td>41</td>
</tr>
<tr>
<td>8.2</td>
<td>Signal Update Time (tU)</td>
<td>41</td>
</tr>
<tr>
<td>8.3</td>
<td>Input Response Time (tIR)</td>
<td>42</td>
</tr>
<tr>
<td>8.4</td>
<td>Output Response Time (tOR)</td>
<td>43</td>
</tr>
<tr>
<td>8.5</td>
<td>System Response Time (tSR)</td>
<td>44</td>
</tr>
<tr>
<td>9</td>
<td>BUS CABLE AND CONNECTOR SPECIFICATIONS</td>
<td>45</td>
</tr>
<tr>
<td>9.2</td>
<td>SERIPLEX Connectors</td>
<td>47</td>
</tr>
<tr>
<td>10</td>
<td>USER DOCUMENTATION</td>
<td>51</td>
</tr>
<tr>
<td>11</td>
<td>GLOSSARY</td>
<td>53</td>
</tr>
</tbody>
</table>
Appendix A—Messaging Protocol .......................... 63
INTRODUCTION ................................................... 63
GLOSSARY .......................................................... 63
DATA TRANSMISSION .......................................... 64
NETWORK ACCESS AND ADDRESSING ....................... 65
MESSAGE STRUCTURE ........................................... 67
Host Messaging Protocol in a Master/Slave Configuration ...... 67
OBJECT ADDRESSING PROTOCOL ......................... 68
FRAGMENT DATA VERIFICATION: THE CRC FIELD ........... 70
COMPATIBILITY OF MESSAGING
WITH MESSAGE-INCAPABLE NODES ......................... 70
1. INTRODUCTION

The SERIPLEX® control bus is a component-level network that provides a simple, inexpensive, fast, and deterministic means of exchanging data among control devices. All control devices are networked together by a single, four-conductor cable, saving the considerable installation cost of traditional hard-wired control and I/O systems. Bus devices include:

- Sensors (photo switches, proximity sensors, and pushbuttons)
- Actuators (valves and contactors)
- Universal input/output modules
- Controllers (PLCs and personal computers)

This document provides sufficient detail to allow designers of control and monitoring devices to create circuits capable of supporting all control bus features. Any device that fully complies with the SERIPLEX standards will coexist and perform at least elementary data exchange with any other compliant device through a control bus. This specification defines the physical and operating characteristics of the control bus, including:

- Signal definitions
- Data transmission methods
- Physical characteristics of the bus and devices
- Signal transmission media
- Behavioral specifications
- Data definitions

This document also includes a glossary of terms and definitions in the back.

This specification describes the second generation of SERIPLEX control systems and devices—systems that are compatible with the SERIPLEX ASIC2B integrated circuit (chip). Requirements for first-generation systems and the ASIC1 chip are not included in this document; however, specific similarities and differences between first and second-generation systems are noted.

The SERIPLEX Standards Specification is the controlling document for SERIPLEX control bus technology. Any device claiming compliance must meet all specifications presented within this document. Unless otherwise noted, all specifications within this document are considered SERIPLEX standards, and must be met by any SERIPLEX device or system. However, some specifications are noted as recommended practices; following these practices is not strictly necessary to ensure SERIPLEX standards compliance, but does help to ensure consistency and interoperability among SERIPLEX devices and systems.

The information contained in this document is protected by US patent number 4808994, which is held by Square D Company. Square D Company reserves all rights to SERIPLEX technology, but has granted full license of this technology to SERIPLEX Technology Organization, Inc. Any use of SERIPLEX technology described in this document or elsewhere without the express, written consent of either Square D Company or the SERIPLEX Technology Organization is prohibited.

1.1. Reference Documents

- SERIPLEX Technology Organization ASIC2B Data Sheet (8310PD9601)
- EN61000-4-1 Electromagnetic Compatibility (EMC)—Part 4: Testing and Measurement Techniques—Section 1: Overview of Immunity Tests
- EN61131-2 Programmable Controllers—Part 2: Equipment Requirements and Tests
1.2. Technical Philosophy

The primary purpose of the SERIPLEX control bus is to replace ordinary wire as a means of transmitting control and data signals among sensing and actuating devices, in a wide variety of applications including industrial control and automation, material handling, facilities automation, and data acquisition.

The main reason for replacing wire is to reduce the installation cost of a control system. Ordinary wiring contributes a significant amount of a typical control system’s installed cost, due to the considerable labor required to pull, label, strip, terminate, and connect wires among large numbers of control and sensing devices within an application. The control bus is intended to reduce control system installation costs by reducing the amount of labor required to physically distribute control signals among control and sensing devices.

Ultimately, the installation labor associated with wiring represents wire’s only truly significant drawback as a technology. A technology intended to replace wire must retain as many of the desirable features of wiring technology as possible, while reducing installation labor and cost as much as possible.

The desirable features of ordinary wire include:

- Fast, predictable, and consistent signal transmission time
- High flexibility of interconnection methods and topology
- High data-handling capacity for discrete signals—to add more signals, add more wires
- High potential resolution of analog signals
- Simplicity of installation—easy to understand and to work with
- Little intelligence or complexity required of the connected devices
- Little or no configuration required of devices or device communication
- Low per-unit cost
- No communications overhead—no signal transmission time is wasted

The need to retain the desirable features of ordinary wiring while reducing the installation cost of control systems led to the establishment of design criteria for the control bus. These design criteria, described below, were used to generate the technology specifications contained within this document:

- Minimize the amount of labor and material required to physically distribute control and data signals among devices
- Keep costs of devices, cable, and controllers as low as possible, subject to the requirements of reduced installation labor costs
- Achieve complete determinism of signal transmission time:
  - Predictable
  - Repeatable
  - Reliable in the presence of electromagnetic interference
- Minimize signal update and response time:
  - Avoid communications overhead to the fullest extent possible
  - Allow flexibility in data packet size and bus speed to minimize response time for a given system size
2. SYSTEM ELEMENTS

- Maximize flexibility of interconnection:
  - Cable length
  - Cable topology
- Keep technology simple to reduce demands on:
  - Device intelligence and cost
  - Personnel training
  - Troubleshooting
  - Bus and device configuration
- Maximize signal capacity:
  - Amount of signals
  - Number of connected devices
  - Length and resolution of signal values
- Perform in industrial environments:
  - Operate reliably in presence of electrical noise
  - Emphasize error avoidance as more efficient than error correction
  - Provide error detection and correction options for extreme applications

Figure 1: SERIPLEX Control Bus System Diagram

A control bus system consists of the following elements, shown in Figure 1:
- Bus cable
- Clock source
- Input and output (I/O) devices
- Bus power supply
- Control power supplies
- Host controller (optional)
The control bus cable conducts bus power and signals among the various system elements. It typically consists of four insulated conductors, surrounded by a shield and an outer insulating jacket. Two of the wires conduct bus power, while the other two conduct a clock and a data signal, used to transmit data among system devices.

The clock source generates the bus clock signal, which synchronizes data transfer among system devices. The clock source also provides a current source for the data signal, so that this signal assumes a normally-high logic state. The clock source periodically transmits a bus fault detect (BFD) pulse that is used by input and output devices to validate the operational status of the bus; the clock source also makes use of this pulse to monitor and report bus fault conditions. The clock source can either be a passive device, providing bus arbitration, or it can be a master, or host controller, providing centralized control and reporting of all bus data.

I/O devices carry out the physical activities of a control system. They can be simple devices like switches and lamps, or complex such as operator-interface terminals and motion controllers. Input devices sense external conditions and report them to the bus, while output devices perform some action based on bus data. I/O devices usually contain a SERIPLEX ASIC2B network interface chip to provide the interface between external signals and the SERIPLEX control bus.

The bus power supply provides power for the bus communications circuitry within each bus device. The bus power supply normally provides a 24-Vdc source for the bus. Multiple bus power supplies can be used within a single system. In general, the bus supply does not provide power to monitoring and control devices, so that an I/O fault would not cause a bus power supply failure, and in turn halt the operation of the bus.

Control power supplies provide power for I/O circuitry such as sensors and actuators. Although this type of power supply can also connect directly to SERIPLEX I/O devices, such supplies typically are electrically isolated from the bus power supply. As a result, control faults such as a shorted load do not affect the operation of the bus itself, although they may trip circuit breakers or otherwise remove power from the control devices.

A host controller typically consists of a combination of hardware and software—for instance, a personal computer or programmable controller—and provides centralized reporting and control of bus data. A host controller usually operates a bus in the master/slave mode, meaning that all bus input data is reported exclusively to the host, and that the host has exclusive control over the states of all bus output signals. Although a host controller is not necessary to operate a bus in the peer-to-peer mode, the majority of control systems do incorporate a host controller.

3. DATA TRANSMISSION

The control bus operates in either of two modes—master/slave or peer-to-peer. Although a host controller can be used in either operating mode, it would typically be used as a master device.

3.1. Peer-to-Peer Mode Data Transmission

In the peer-to-peer bus operating mode, bus input and output data can be shared directly among devices. Although a host controller can be used in this mode, it would not necessarily have exclusive control of bus output data, nor would it have exclusive access to bus input data. More typically in the peer-to-peer mode, a simple clock source would be used to provide bus arbitration functions, but this device would not perform supervisory control.
SERIPLEX data is transmitted by means of the bus clock and data signals. Normal bus operation consists of a scanning process, wherein frames of bus data are transmitted repeatedly, so that all bus data signals are updated periodically at a set frequency. Each data transmission frame is defined by a series of pulses on the clock line, separated by sync periods during which the clock line remains inactive (see Figure 2).

Each clock period corresponds to an address. In the peer-to-peer mode, each address corresponds to exactly one bit of signal information. Addresses are numbered from 0 to 255; clock pulses are numbered correspondingly. After each sync period, a new series of clock pulses is transmitted starting with the falling edge of pulse number 0, and continuing incrementally until the data frame is complete and the next sync period begins.

During each clock period, the corresponding bus data signal is reported to the bus through the data line. The data line normally rests at a logic-high level, which corresponds to a data value of 0; a device can pull the data line low during a clock period to assert a data value of 1 for the corresponding signal.

Every device that communicates through the SERIPLEX control bus is assigned to at least one address. Devices can be assigned to multiple addresses; in fact a host controller can be considered to be assigned to every available address. A device’s assigned addresses may or may not be contiguous, but individual multi-bit data values (for instance, a 16-bit analog signal) must be assigned at least enough contiguous addresses to accommodate their value range.

In the peer-to-peer mode, each address used must be assigned to at least one input device and one output device for communication to occur. In other words, every bit of data sent through the bus must be received by some device; otherwise, transmission of that bit serves no control purpose. In some cases, a host controller may be the only designated sender or receiver of a given data signal. To arrange direct control of an output device by an input device, those devices are assigned the same address (or addresses).

Each device on the network counts the clock pulses within each data frame, and monitors and/or controls the state of the data line during the clock periods corresponding to the device’s assigned signal addresses. During clock periods which do not correspond to the assigned signal addresses, a bus device does not attempt to pull the data line low, nor is its operation affected by the state of the data line.

The maximum number of clock pulses per data frame is 256; and address 0 cannot be used by any bus device. Therefore, the maximum data capacity within a single peer-to-peer mode data frame is 255 bits. Since each address is used as both an input and an output signal, this represents an I/O capacity of 255 discrete (single-bit) inputs and 255 discrete outputs, for a total of 510 I/O devices.
3.2. Master/Slave Mode Data Transmission

In the master/slave bus operating mode, all bus input data is reported exclusively to the master, and the master has exclusive control over the states of all bus output signals, with all bus I/O devices acting as slaves. In almost all cases, master/slave mode systems use a host controller that acts as both the clock source and as the bus master device. See Figure 3 for the master/slave data transmission format.

Figure 3: Master/Slave Mode Data Transmission

Master/slave mode data transmission is similar to that of the peer-to-peer mode in most respects. The most significant difference is that in the master/slave mode, there are two clock pulses per signal address instead of one. During the first clock pulse for each address, the corresponding bus input signal is reported, and the corresponding bus output signal is reported during the second clock pulse. In this mode, bus devices divide the number of clock pulses by 2 to determine the currently-active signal address.

Since bus input and output signals are reported at different times, input signals do not exert direct control over output signals that share the same address, as they would in peer-to-peer mode; in fact, such input/output signal pairs can be completely unrelated in the control logic. This is true even if the input and output signals that share an address reside within the same SERIPLEX device. In master/slave mode, the state of bus output signals is exclusively under the control of the bus master. Note, however, that bus masters can include a pass-through feature to logically link input and output signals at the same address, so that peer-to-peer mode operation can be imitated for any or all signal addresses.

This logical separation of bus input signals and output signals at the same address allows the master to make all control decisions and to have exclusive control over the state of all bus output signals. Slave devices report bus input data, but they do not monitor the states of bus input signals. All bus output data is transmitted exclusively by the bus master; slave devices can monitor output data signals, but they do not produce them.

Since the master/slave mode uses two clock pulses per address, the maximum number of clock pulses per frame is 512. Therefore, master/slave mode takes roughly twice as long as peer-to-peer mode to scan the same number of I/O addresses. As in peer-to-peer mode, address 0 cannot be used by any bus device. Therefore, the I/O capacity for master/slave mode is the same as for peer-to-peer mode—255 discrete inputs and 255 discrete outputs.

All other aspects of master/slave mode data transmission are identical to those of peer-to-peer mode.
3.3. General Data Transmission

Features

3.3.1. Address Multiplexing

The following sections describe operational characteristics of data transmission that are applicable to both peer-to-peer and master/slave bus operating modes.

The data capacity of a single data frame is 255 input bits and 255 output bits. While this is a considerable capacity for discrete I/O devices, the number of analog signals within a single frame is limited to 15 (16-bit) inputs and 15 outputs, which is not sufficient for many applications.

Address multiplexing is a means of expanding the data capacity of a control bus. In address multiplexing, multiple devices share the same signal addresses. Individual signals at the shared addresses are distinguished by assigning each to one of 16 unique multiplex channels. Each data frame transmits data for a single multiplex channel. Using the multiplex channel extends the addressing range of the SERIPLEX control bus from 8 bits to 12 and results in an increase in a single bus’s data capacity from 510 signal bits to 7,680 signal bits, a factor of approximately 15.

Each multiplexed device monitors the multiplex channel indication at the beginning of each data frame and determines whether the device’s assigned channel number. If a device’s assigned channel is being scanned, that device reads and writes bus data normally. However, if the current channel does not correspond to that device’s assigned channel, the device ignores bus output data and does not transmit its bus input data within that data frame.

The clock source indicates the currently active multiplex channel using output signals 1–4. These four signals form a binary number indicating a multiplex channel between 0 and 15, with output 1 indicating the least significant bit of the channel number. Multiplexed devices compare the value of these four bits to their assigned multiplex channels to determine whether their signals are active within that data frame. See Figure 4 for multiplex channel format.

Address multiplexing is performed on words composed of 16 contiguous addresses, located at 16-bit address boundaries (16–31, 32–47, ..., 240–255). In order to multiplex any individual address, the entire 16-bit word in which it resides must be multiplexed.

The word starting at address 0 is not multiplexed, since that word contains the multiplex channel indication. This leaves 15 multiplexable address words.

In master/slave mode, there are 15 multiplexable input data words and 15 multiplexable output data words. This supports a total of 480 multiplexed data words (15 words x 16 channels x 2 input/output), or 7,680 individual data bits.

If address multiplexing is used within a system, it is not necessary to multiplex all addresses. Multiplexing can be selected for individual words and not selected for others. There are no restrictions or requirements for which words are multiplexed within a system. In master/slave mode, input and output words can be multiplexed differently—for example, input word 16–31 can be multiplexed even if output word 16–31 is not.

### Table 1: Multiplex Channel Indication

<table>
<thead>
<tr>
<th>Output Signals</th>
<th>Non-Multiplexed Data</th>
<th>Multiplexed Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Non-multiplexed devices simply ignore the multiplex channel indication, and report and receive their data within every data frame. Obviously, multiplexed and non-multiplexed signals cannot share the same addresses, since this would result in data contention during multiplex channels assigned to multiplexed signals.

Since multiplexed signals are only updated during data frames that correspond to their assigned multiplex channels, multiplexed signal update time is related to the number of multiplex channels and the order in which they are scanned. The update time for multiplexed signals is typically calculated as \([(frame\ time) \times (number\ of\ multiplex\ channels)\] , although some applications may vary from this formula. Note, however, that non-multiplexed signals are still updated once per data frame, even in systems that use address multiplexing at other signal addresses.

It is recommended practice to scan multiplex channels in ascending numerical order and then repeat. However, there are no set requirements on the order of multiplex channel scanning; multiplex channel scan order can be customized within an application to allow prioritizing of signal update times. For instance, a host controller can support a priority channel that is scanned every second data frame, while other multiplex channels are scanned in ascending numerical order in between each priority channel frame.

Any number of multiplex channels can be used within a system, up to the maximum of 16.

SERIPLEX systems that use address multiplexing cannot assign output signals 1 through 4 to an output device, since these bits are used for multiplex channel indication. The recommended practice is to avoid assigning any address within the first word (addresses 0 through 15) to any I/O device, except for dedicated functions noted elsewhere within this specification.

Each multiplexed signal is assigned to a single multiplex channel. However, an I/O device that transmits and/or receives multiple signals can have different signals assigned to different multiplex channels. For instance, a four-point analog input module can have each of its four signals assigned to addresses 48 through 63, with individual signals assigned to multiplex channels 0, 1, 2, and 3.

### 3.3.2. Sync Period

The sync period is a period of inactivity on the bus clock line, which is detected by all bus devices and used to reset their internal address counters at the start of each data frame. It is measured from the positive (low-to-high) bus clock signal transition at the end of a data frame to the negative (high-to-low) clock transition that begins the next data frame (see Figure 5).

The timing of the sync period is controlled by the clock source. Once all clock pulses for a given data frame have been completed, the clock source holds the bus clock line high for the duration of the sync period.

The minimum and maximum sync period durations are selected to ensure that I/O devices can reliably detect the presence of a sync period over the bus clock rate range of 10 to 200 kHz, without interpreting the inactivity as a loss of the bus clock signal.

Although the clock source does not generate clock pulses during the sync period, the clock period is usually still used as the unit of time measurement for events that occur within the sync period. The recommended practice for sync period duration is 8.5 clock periods for clock rates up to 100 kHz, and 16.5 clock periods for clock rates greater than 100 kHz.
Upon detection of a sync period, I/O devices reset their address counters to 0 in preparation for the next data frame; and monitor the bus data line for the presence of a bus fault detection pulse, to determine their appropriate output responses upon the end of the sync period.

![Figure 5: Sync Period Diagram](image)

**Table 2: Sync Period Parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Minimum</td>
</tr>
<tr>
<td>(t_{\text{clock}})</td>
<td>Clock period</td>
<td>—</td>
</tr>
<tr>
<td>(t_{\text{sync}})</td>
<td>Sync period duration</td>
<td>82 (\mu\text{s})</td>
</tr>
<tr>
<td>(t_{\text{bd}})</td>
<td>BFD pulse duration</td>
<td>(2 \times t_{\text{clock}} - 0.5 \mu\text{s})</td>
</tr>
<tr>
<td>(t_{\text{pd}})</td>
<td>BFD pulse delay time</td>
<td>(t_{\text{clock}} - 0.5 \mu\text{s})</td>
</tr>
<tr>
<td>(t_{\text{br}})</td>
<td>BFD pulse recovery time</td>
<td>(2 \times t_{\text{clock}} - 0.5 \mu\text{s})</td>
</tr>
</tbody>
</table>

### 3.3.3. Bus Fault Detection Pulse

The bus fault detection (BFD) pulse is a negative pulse on the bus data line during the sync period, which is used by both the clock source and I/O devices to determine the health of the control bus. See Figure 5.

As at other times, the bus data line rests at a normally-high logic state during the sync period. During each sync period, the clock source pulls the data line low, and then releases it high again before the end of the sync period, to create the BFD pulse.

The clock source monitors the data line during and after the BFD pulse to determine whether the data line can be driven to both logic-high and logic-low states. If the data line fails to reach either the logic-high or -low state, the clock source recognizes a bus fault and halts the transmission of the clock signal.

Each I/O device on the SERIPLEX bus monitors for the presence of the BFD pulse during each sync period. If the BFD pulse is detected and the sync period ends normally, the I/O device presumes that the bus is operating properly and allows bus output data received during the previous data frame to be transmitted to its external output signals, subject to any other fault-detection mechanisms that the device uses. If the device fails to detect a BFD pulse during a sync period, the device recognizes a bus fault condition, and its external output signals revert to their default (shelf) state.

The BFD pulse must fall entirely within a sync period. The pulse’s transition from a logic-high to a logic-low state must occur after the bus clock line has reached the logic-high state at the start of the sync period and after the minimum BFD pulse delay time, specified in Table 2, has elapsed. The pulse’s transition from logic-low to logic-high must precede the clock line’s first high-to-low transition, in the following data frame, by the minimum BFD pulse recovery time (specified in Table 2).
There are no exact requirements for BFD pulse duration or for its position within the sync period. The recommended practice is for the BFD pulse to be exactly two clock periods in duration, and for it to occur during the second and third equivalent clock periods within the sync period.

**NOTE:** The bus fault detection pulse provided by the version 1 SERIPLEX control bus clock sources was not standardized, and was implemented in several different ways. Version 1 SERIPLEX control bus I/O devices required only a positive transition of the bus data line within the sync period.

### 3.3.4. Frame Length

Frame length is the number of addresses scanned within a data frame. The frame length sets the number of individual bus input or output signal bits that are reported within a data frame.

The frame length can be any number up to a maximum of 256. Recommended practice is that frame length be a multiple of 16 (16, 32, 48, ..., 240, 256), and that the frame length be constant within a given system.

In the peer-to-peer mode, the frame length is equal to the number of clock pulses produced within a data frame. In the master/slave mode, the number of clock pulses is twice the frame length. Therefore the frame length directly affects signal update time, since it determines the duration of a data frame for a given clock rate.

The number of available addresses within a data frame is \([\text{frame length} - 1]\), since Address 0 is not usable. For instance, a frame length of 64 supports up to 63 bus input signal bits and 63 output bits.

### 3.3.5. Clock Rate

The bus clock rate is the frequency at which bus clock pulses are transmitted during the data-transmission portion of a data frame. This can be any value between 10 and 200 kHz. Recommended nominal values (in kHz) are 10, 12, 16, 20, 25, 32, 50, 64, 75, 100, 125, 150, 167, and 192.

For a given frame length, the clock rate determines the duration of a data frame, and so determines signal update and response times. The clock rate also affects the number of I/O devices that can be connected to a single bus cable, and the total cable length within a system, by establishing the maximum allowable charging time of the bus data line (see "4.5. Signal Timing" on page 23 for more details).

**NOTE:** The definition of clock rate excludes the sync period portion of a data frame. Therefore, direct measurement of the clock rate by a frequency counter connected to the bus clock line may produce an inaccurate value, since the presence of sync periods reduces the observed frequency.

**NOTE:** Version 1 SERIPLEX control bus systems supported clock rates only from 10 to 100 kHz.

### 3.3.6. Data Length

The length of a data signal transmitted through a control bus can range from a single bit up to 255 bits. Recommended signal data lengths are 1, 2, 4, 8, 16, or any multiple of 16 bits up to 240.

Any signal longer than one bit must be assigned at least as many contiguous addresses as are required to accommodate the data value in binary form. If the assigned address space exceeds the data length, the recommended practice is for the signal-producing device to transmit signal values of 0 for the unused bits.

### 3.3.7. Address Sharing

Multiple SERIPLEX devices can be assigned to the same signal address or addresses. In fact, in the peer-to-peer mode, at least two devices—one input device and one output device—must be assigned to the same signal address for the associated signal to perform any useful communication.
In addition to input/output signal pairs, multiple input devices can also share an address. In this way, any of several input devices can produce the same input signal. The input signal is the logical OR combination of all input devices assigned to that address; this is frequently referred to as a wire-OR logic function. The recommended practice is to assign only discrete (single-bit) signals to a shared address; multi-bit signals (such as analog values) should not share addresses, except as allowed under the rules for address multiplexing.

Similarly, multiple output devices can also share an address. The output signal controls all associated output devices in exactly the same way; this is referred to as a wire-AND logic function. Again, only single-bit signals should share addresses, except in the case of multiplexing.

There is no set limit on the number of devices that can share addresses, although practical constraints are imposed by the physical limits of a system.

The SERIPLEX control bus address-sharing capability enables the address multiplexing feature of the bus. In address multiplexing, multiple devices and signals share the same address space, but only one signal is active during a given data frame. See section “3.3.1. Address Multiplexing” on page 11 for more information.

There are no physical or protocol constraints that would prevent an I/O device from operating at any valid address from 1 through 255, providing that enough addresses are assigned for a multi-bit signal. However, the recommended practice is to assign starting addresses for signals of given data lengths as follows:

- Assign 1-bit signals to any valid address
- Assign 2-bit signals to an even-numbered address (2, 4, 6, etc.)
- Assign 3- or 4-bit signals on 4-bit address boundaries (4, 8, 12, etc.)
- Assign 5- to 8-bit signals on 8-bit address boundaries (8, 16, 24, etc.)
- Assign signals of more than 8 bits on 16-bit address boundaries (16, 32, 48, etc.)

In particular, multiplexable devices must be assigned starting addresses that are multiples of 16.

NOTE: These address assignments may result in some wasted addresses that are not used to carry actual data signals. However, assigning signal addresses according to these guidelines usually reduces the data processing requirements of host control software.

3.3.8. Device Address Boundaries

4. BUS PHYSICAL CHARACTERISTICS

4.1. Bus Power

The following sections describe essential physical characteristics of control bus system components.

4.1.1 Voltage and Current Levels

The bus power supply provides power for the SERIPLEX bus communications circuitry within each bus device. The bus power supply normally provides a 24-Vdc source for the bus. Multiple bus power supplies can be used within a single SERIPLEX control bus system. In general, the bus supply does not provide power to monitoring and control devices, to prevent an I/O fault from causing a bus power supply failure and in turn halting the operation of the bus.

The control bus operates from a 24 Vdc nominal source, with the positive voltage connected to the bus power conductor, and the negative lead connected to the bus common conductor. Power supply requirements are summarized in Table 3.
NOTE: Version 1 SERIPLEX control bus systems required a 12 Vdc nominal supply (range 10.5 to 13 Vdc). Version 2 devices can support this voltage range also, but it is not required.

Bus power must not operate in the range of 15 to 19.2 Vdc, because this is the EEPROM programming voltage range of the SERIPLEX control bus ASIC2B chip.

Bus power supply current output requirements are not fixed, but rather are dependent upon the current draw of SERIPLEX devices installed within a given system. The bus power supply must be capable of providing sufficient current to drive the bus power loads of all connected bus devices, while holding bus power voltage and ripple within the specified levels.

Bus power supply input or line regulation requirements are not fixed. However, the bus power supply must be capable of holding bus power voltage and ripple within specified levels through worst-case variations of a given system’s line voltage, including any user-specified requirements for brownout or dropout conditions.

Bus power specifications must be met at all device connection points within a bus system. Therefore, the bus power supply voltage must be set to a sufficient level to compensate for any voltage drops that may exist through the bus cable.

The bus power supply must be capable of supplying specified voltage levels through the SERIPLEX bus cable to all connected devices. In cases where the voltage drop through the bus cable would reduce the supply voltage or shift the common potential at remote I/O devices outside specified levels, it may be necessary to install multiple bus power supplies within a single SERIPLEX system.

In systems where multiple bus power supplies are used to ensure proper bus voltage to all devices, the recommended practice is to connect together the common conductors of all the supplies, and to isolate the power conductors from separate supplies. Connecting the common conductors provides a common reference for the bus clock and data signals. Isolating the different supplies’ power conductors serves two purposes:

- It eliminates the possibility of contention among supplies that are not adjusted to identical voltage levels.
- It can allow portions of the SERIPLEX system to continue operating despite the failure of a single bus power supply, since the failed supply does not exert a load on the other bus power supplies.

Multiple bus power supplies can also be used to provide redundancy, allowing the SERIPLEX bus to continue operating despite the failure of a bus power supply. In this case, the recommended practice is to connect the positive conductors of all redundant bus power supplies to the bus power line through isolating diodes, thus preventing a failed supply from presenting a load to other connected bus power supplies.

Connecting the positive conductors of multiple bus power supplies directly to the same SERIPLEX control bus power line (without isolating diodes) is not a recommended practice.

Table 3: Power Supply Requirements

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum voltage</td>
<td>30.0 Vdc (including ripple)</td>
</tr>
<tr>
<td>Minimum voltage</td>
<td>19.2 Vdc (including ripple)</td>
</tr>
<tr>
<td>Maximum ripple</td>
<td>1.2 V peak-to-peak</td>
</tr>
</tbody>
</table>

4.1.2. Power Distribution
This Standard Specification makes no explicit requirements regarding the location of bus power supplies. In general, it is expected that bus power supplies will be located so as to limit the maximum bus cable distance between the bus power supply and remote I/O devices.

4.1.3. Device Power Consumption

Current consumption requirements for SERIPLEX devices are not specified explicitly, due to the flexibility and variability of SERIPLEX control bus applications. However, in general, recommended practice is to minimize the I/O device’s current draw from the bus power line.

The bus power supply must be capable of providing sufficient current to drive the bus power loads of all connected bus devices, and to accommodate all variations in bus power loading, while holding bus power voltage and ripple within the specified levels. Smaller and less-variable device current consumption eases the requirements of a given system’s bus power supply. Device power consumption requirements during device set-up are defined in “7. Device Programming” on page 40.

4.1.4. Load Regulation

Bus power supply load regulation requirements are not fixed, but rather are dependent upon the current draw of connected bus devices. Some systems may have a nearly constant current draw, while others may see wide variability in loads. The bus power supply must be capable of holding bus power voltage and ripple within specified levels through the worst-case load transition of a given system.

4.1.5. Isolation

It is highly desirable to isolate the SERIPLEX system’s bus power and signals from all other control circuits for a variety of reasons, including:

- Reduced conduction of voltage surges, current spikes, dv/dt transients, and other electromagnetic disturbances onto the SERIPLEX bus cable, where such disturbances could interfere with proper bus data transmission and/or damage bus devices
- Reduced probability that a failure of an I/O device or of control power will reduce the bus voltage or otherwise cause the SERIPLEX bus to cease operating properly
- Reduced loading and variability of the SERIPLEX power supply
- Simpler design and implementation of proper SERIPLEX control bus shielding and grounding

SERIPLEX control bus I/O devices and clock sources isolate their external input and output signals from the bus power and signals, except as noted within this section. Most devices accomplish this isolation through optical coupling devices. Isolated devices must be capable of withstanding 500 Vac applied between the SERIPLEX bus conductors and any I/O connection points for a minimum of one second; 1500 Vac is recommended.

Using SERIPLEX bus power for circuitry other than bus communication circuitry is prohibited, except under the following conditions:

- Such circuitry is not galvanically connected to any other power source or supply circuit
- Such circuitry and all devices connected to such circuitry are not exposed to electrical or electromagnetic disturbances that could be conducted into the bus device and interfere with the operation of the control bus
- The load presented by the device to the bus power supply during normal operation does not vary by more than 100 mA, including changes induced by changing signal states
Any internal device power supply that draws current from the bus power supply must be overload-protected, so that a short or overload condition on the device supply’s output does not result in excessive current draw from the bus power supply.

The following types of devices can make use of the bus power supply, provided that the conditions listed above are met:

- Electromechanical input devices such as limit switches, pushbuttons, or selector switches
- Solid-state sensors (such as photoelectric, inductive, and capacitive)
- LED indicator lamps

The following devices must isolate bus connections from their external I/O signals:

- Contactors, solenoids, valves, and other types of large inductive loads
- Switches and sensors that use another control power source such as a 120-Vac or another 24-Vdc supply
- Incandescent lamps

### 4.2. Data Line Characteristics

The bus data line is driven by a 30 mA current source within the clock source, so that it normally rests at a logic-high level of approximately 12.0 Vdc, as referenced to the bus common line. Table 4 summarizes the data line characteristics.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>High signal voltage at clock source</td>
<td>11.4 Vdc</td>
<td>12.0 Vdc</td>
<td>14.0 Vdc</td>
</tr>
<tr>
<td>High signal voltage at I/O device</td>
<td>9.2 Vdc</td>
<td>12.0 Vdc</td>
<td>16.2 Vdc</td>
</tr>
<tr>
<td>Source current</td>
<td>27 mA</td>
<td>30 mA</td>
<td>33 mA</td>
</tr>
<tr>
<td>Logic-high threshold</td>
<td>6.75 Vdc</td>
<td>7.50 Vdc</td>
<td>8.25 Vdc</td>
</tr>
<tr>
<td>Logic-low threshold</td>
<td>2.7 Vdc</td>
<td>3.0 Vdc</td>
<td>3.3 Vdc</td>
</tr>
<tr>
<td>I/O device leakage current (at logic low)</td>
<td>—</td>
<td>—</td>
<td>30 μA</td>
</tr>
<tr>
<td>I/O device input current draw (at logic high)</td>
<td>—</td>
<td>—</td>
<td>15 μA</td>
</tr>
<tr>
<td>Data driver on-state voltage (@ I\textsubscript{data} ≤ 33 mA)</td>
<td>0.0 Vdc</td>
<td>—</td>
<td>0.7 Vdc</td>
</tr>
</tbody>
</table>

**Figure 6: Data Line Diagram**
The bus data line is low-true—a logic-high level corresponds to a data value of 0, and logic-low level corresponds to 1. The data line rests at the logic-high (0) state and is pulled to logic low when a device asserts a data value of 1 for a particular signal.

Data line logic thresholds incorporate hysteresis to protect against spurious changes in logic state induced by electrical noise or signal reflections. When a device has sensed a logic-high level on the data line, the data line voltage must drop below the logic-low threshold in order for that device to sense a logic-low condition. Similarly, when the data line is sensed as low, it must exceed the logic-high threshold to be sensed as high. See Figure 7.

Figure 7: Hysteresis

The bus data line is sampled at the negative (logic high-to-low) transition of the bus clock signal within each clock period. The state of the data line at other times within the data frame is ignored by all bus devices, including the clock source.

The data line current source sees a complex impedance load, consisting of the bus cable (essentially a transmission line, which includes capacitive effects) and the capacitance of the I/O devices in the system. For short systems, the data line response is dominated by system capacitance, and the line charges at a nearly linear rate. For long systems, the response begins to resemble a stair-step shape, dominated by the cable’s transmission line delay. In either case, the time required to charge the data line to the logic-high threshold determines the maximum clock rate, the number of connected bus devices, and the cable length for a given system. See “4.5. Signal Timing” on page 23.

NOTE: SERIPLEX control bus version 1 logic-high and -low thresholds were set to 75% and 25%, respectively, of the bus power voltage, rather than the fixed 7.5 Vdc and 3.0 Vdc nominal levels specified for version 2.

4.3. Clock Line Characteristics

The bus clock line is driven by a totem-pole driver circuit within the clock source, so that it oscillates between bus common (0 V) and 12 Vdc. Clock line characteristics are summarized in Table 5.
Figure 8: Clock Line Diagram

The clock line oscillates at a 50% duty cycle, at the designated clock rate for a given system.

Clock line logic thresholds incorporate hysteresis to protect against spurious changes in logic state induced by electrical noise or signal reflections. When a device has sensed a logic-high level on the clock line, the clock line voltage must drop below the logic-low threshold in order for that device to sense a logic-low condition. Similarly, when the clock line is sensed as low, it must exceed the logic-high threshold to be sensed as high. See Figure 7.

The clock line normally rests at a logic-high state during the sync period or when the clock signal is halted by the clock source.

NOTE: SERIPLEX control bus version 1 logic-high and low thresholds were set to 75% and 25%, respectively, of the bus power voltage, rather than the fixed 7.5 Vdc and 3.0 Vdc nominal levels specified for version 2.
4. Bus Physical Characteristics

Each SERIPLEX system contains only one bus cable. That is, all segments of bus cable are directly connected together, so that continuity for each individual bus conductor is maintained throughout the entire system. All bus devices are connected in parallel to this single bus cable, as shown in Figure 10. This ensures that when any bus device is disconnected from the cable, continuity is maintained to all other devices in the system.

There are no explicit requirements for the topology of the SERIPLEX bus cable within a system, nor are there fixed limits for the total length of bus cable or number of bus nodes within a system. Cable length and node limits are determined primarily by a system’s clock rate and the total data line capacitance within a system.

Bus cable topology can be any of several types. Recommended topologies are daisy chain or trunk-and-drop (see Figure 11), since their performance is most predictable and easily characterized.
Figure 11: Recommended Bus Cable Topologies

Other topologies can be used, as shown in Figure 12; however, it is the responsibility of the system designer to provide a system that will operate as required under all possible operating conditions.

Figure 12: Alternate Bus Cable Topologies

The maximum length of cable and the maximum number of nodes that can be connected to a single SERIPLEX bus cable are interdependent, and are determined by the following factors:

- Bus clock rate
- Bus data source current
- Data line capacitance per unit of cable
- Data line capacitance per connected node
- Clock and data line resistance per unit of cable
- Power and common line resistance per unit of cable
- Amplitude of ringing due to bus cable reflections and inductance
- Cable propagation delays

The bus clock rate determines the amount of time available to the bus data line when it is required to charge from a logic-low state in one clock period to a logic-high state in the following clock period. The maximum available charging time establishes a limit on the total system capacitance and cable length. In general, increasing the capacitance slows the data line charging process, and increasing the cable length adds to the propagation time necessary for the line charge to be distributed across the entire bus cable. Each segment of bus cable adds to both the distributed capacitance and the cable propagation time, while each additional connected node adds to the capacitance alone. The bus cable and the connected nodes contribute to the overall charging time of the bus, and this charging time must fall within the limit for the designated clock rate. There is no set limit to the length of a branch cable connected to a main trunk cable, although the recommended practice is to limit drop lengths to less than 30 feet, in order to limit ringing due to inductance and signal reflections.
4.5. Signal Timing

Figure 13: Data Signal Timing Diagram

Table 7: Symbols and Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_clock</td>
<td>Clock period</td>
<td>—</td>
</tr>
<tr>
<td>t_pon</td>
<td>Data-on propagation delay</td>
<td>0</td>
</tr>
<tr>
<td>t_off</td>
<td>Data-off propagation delay</td>
<td>0</td>
</tr>
<tr>
<td>t_ch</td>
<td>Data line charge time</td>
<td>0</td>
</tr>
<tr>
<td>t_dis</td>
<td>Data line discharge time</td>
<td>0</td>
</tr>
<tr>
<td>t_setup</td>
<td>Set-up time before data sampling</td>
<td>100 ns</td>
</tr>
<tr>
<td>t_hold</td>
<td>Hold time after data sampling</td>
<td>100 ns</td>
</tr>
<tr>
<td>t_loss</td>
<td>Clock loss detect time</td>
<td>1.3 ms</td>
</tr>
<tr>
<td>t_prog</td>
<td>Programming mode enable time</td>
<td>40 ms</td>
</tr>
</tbody>
</table>

The most fundamental unit of time for SERIPLEX control bus operation is the clock period $t_{clock}$, which is defined as the elapsed time between successive positive transitions of the bus clock signal during the data-transfer portion of a data frame. See Figure 13.

The clock signal is nominally a 50%-duty-cycle square wave, so that one-half clock period elapses between positive and negative transitions of the bus clock signal.

During the data transmission portion of a data frame, the bus clock source transmits a clock pulse for each clock period. During the sync period, clock pulses are not generated, but the clock period is usually still used as the unit of time measurement for events that occur within the sync period.
The positive (logic low-to-high) transition of the bus clock signal triggers both assertion and removal of data signals from the bus data line. A device asserts its data on the data line immediately upon sensing the positive clock transition that begins a clock period corresponding to a signal that the device produces. The device maintains data on the data line until it senses the next positive clock transition, and then releases the data line immediately.

In order for a device to assert a signal value of 1, it must discharge the bus data line to a logic-low level before the negative transition (logic high-to-low) of the corresponding bus clock pulse, with allowance made for the required set-up time ($t_{\text{setup}}$). The available discharge time ($t_{\text{dis}}$) is limited by the device propagation delay ($t_{\text{pon}}$), and the bus cable propagation delay ($t_{\text{pcable}}$). Therefore, in order for a logic-low condition to be sensed by all bus devices, the following condition must be met:

$$t_{\text{pon}} + t_{\text{dis}} + 2(t_{\text{pcable}}) < \left( \frac{t_{\text{clock}}}{2} - t_{\text{setup}} \right)$$

Following a clock period in which the bus data line has been driven low, the data line must recharge to a logic high level before the negative transition of the next bus clock pulse, for devices to sense a logic value of 0. Again, allowance must be made for the required set-up time ($t_{\text{setup}}$); and the available charge time ($t_{\text{ch}}$) is limited by device ($t_{\text{poff}}$) and cable propagation delays ($t_{\text{pcable}}$). The required condition is:

$$t_{\text{poff}} + t_{\text{ch}} + 2(t_{\text{pcable}}) < \left( \frac{t_{\text{clock}}}{2} - t_{\text{setup}} \right)$$

As shown in the formulae above, the bus clock rate determines the amount of time available for the logic level of the bus data line to change. Therefore, the clock rate also determines the node capacity and cable length of a given bus system.

The data line must charge to a logic-high state within the required time following a clock period in which the bus data line has been driven to a logic-low state. Otherwise, bus devices might read a value of 1 for a logic signal with an intended value of 0.

The data line is sampled at the negative transition of the bus clock signal within each clock period during the data-transfer portion of a data frame. The clock loss detect time ($t_{\text{loss}}$) is the minimum elapsed period, without a negative transition of the bus clock signal, that devices will interpret as absence of the clock signal, rather than a sync period.

The programming mode detect time ($t_{\text{prog}}$) is the minimum time that must elapse, while the bus clock line remains high, before a bus I/O device will enter the programming mode.

**NOTE:** SERIPLEX control bus version 1 clock loss detect time ranged from 40 to 170 ms, as compared to 1.5 ms nominal for version 2.
4.6. Environmental Requirements

All SERIPLEX devices must meet the minimum requirements for electromagnetic compatibility given in Table 8, as applied to the bus circuitry. EMC requirements for other device circuitry (such as I/O points) are left to the discretion of the device vendor.

**Table 8: Minimum Requirements**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Bus Power Supply</th>
<th>Data Lines</th>
<th>Device Enclosure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge immunity EN61000-4-2</td>
<td>level 1 2 kV air, contact</td>
<td>level 3 8 kV air, 6 kV contact</td>
<td>level 1 2 kV air, contact</td>
</tr>
<tr>
<td>Radiated electromagnetic field EN61000-4-3</td>
<td>—</td>
<td>—</td>
<td>level 3 8 kV air, 6 kV contact</td>
</tr>
<tr>
<td>Electrical fast transient burst EN61000-4-4</td>
<td>level 1 0.5 kV</td>
<td>level 3 2 kV</td>
<td>level 1 0.25 kV</td>
</tr>
<tr>
<td>Surge immunity EN61000-4-5</td>
<td>installation class 0 (no levels)</td>
<td>inst. class 2 1 kV line-to-earth, 0.5 kV line-to-line</td>
<td>inst. class 2 1 kV line-to-line</td>
</tr>
<tr>
<td>Conducted RF EN61000-4-6</td>
<td>—</td>
<td>level 3 10 Vrms</td>
<td>level 3 10 Vrms</td>
</tr>
<tr>
<td>Impulse immunity IEC60255-4</td>
<td>class 2 1 kV</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

1. Capacitive coupling only.

There are no explicit requirements for the physical environment in which a SERIPLEX device is installed, other than the electromagnetic characteristics given above. However, Table 9 lists the recommended practices for minimum environmental tolerance levels for any SERIPLEX device intended for use in an industrial application.

**Table 9: Minimum Environmental Tolerance**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature range</td>
<td>0 to +60 °C (32 to 140 °F)</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>-25 to +85 °C (-13 to +185 °F)</td>
</tr>
<tr>
<td>Relative humidity</td>
<td>5 to 95%, non-condensing</td>
</tr>
<tr>
<td>Airborne pollutants</td>
<td>IEC60664-1, Section 2.5.1</td>
</tr>
<tr>
<td>Operating shock</td>
<td>EN60068-2-27</td>
</tr>
<tr>
<td>Operating vibration</td>
<td>EN60068-2-6</td>
</tr>
</tbody>
</table>

5. DATA DEFINITIONS

The following sections describe conventions for the formulation and interpretation of data transmitted through the control bus. In accordance with the SERIPLEX control bus technical philosophy of maintaining maximum system flexibility, most of these conventions are recommended practices rather than explicit requirements. Within any given SERIPLEX control bus system, data can be defined and used in any manner suitable to that system’s purpose, provided that there is not conflict among devices in the use or meaning of any given data signal.

5.1. Special Signal Definitions

In accordance with the SERIPLEX bus technical philosophy of maintaining maximum system flexibility, no set restrictions are placed on the meaning of data transmitted through the control bus. However, the following sections list recommended conventions for the meaning of bus data. These conventions should be followed to the extent possible within any given SERIPLEX system.
5.1.1. Address 0

Input signal 0 and output signal 0 cannot be used to transmit data among SERIPLEX devices. Physically, bus clock pulse 0 is not usable by SERIPLEX devices because its negative transition, upon which data would be sampled, is not preceded by a positive transition; this preceding positive transition would be necessary to instruct any signal-transmitting device to assert a signal on the bus data line in advance of the negative clock signal transition.

5.1.2. Multiplex Channel Indication

Outputs signals 1–4 are used by a clock source to indicate the multiplex channel to be updated within the current data frame.

Within a master/slave mode system, outputs 1–4 cannot be used for any other purpose without interfering with the multiplex channel indication. Within a peer-to-peer mode system, neither inputs 1–4 nor outputs 1–4 can be used, as these signals occupy the same bus clock periods.

The multiplex channel indication is a four-bit binary number, with the least significant bit corresponding to output 1 and the most significant to output 4.

5.1.3. Data Echo Signals

Application designers have the choice of designating SERIPLEX bus input signals as data echo signals. When designated in such a way, the input signal represents the state of a SERIPLEX bus output signal, as received by a given bus device, rather than an ordinary bus input signal generated by the bus device. For details, refer to “6.6.2. Data Echo” on page 31.

5.1.4. Complementary Data Retransmission (CDR) Signals

Application designers have the choice of designating SERIPLEX bus input and output signals as complementary data retransmission (CDR) data. When designated in such a way, a signal does not represent actual control signal data, but instead represents an encoded version of a control data signal. For details, see “6.6.3. Complementary Data Retransmission (CDR)” on page 31.

5.2. Signal Addressing Conventions

The following are recommended practices for the assignment of signal addresses to devices:

- Signal addresses from 0 through 15 should not be used to transmit I/O data within a SERIPLEX system. These addresses should be reserved for designated system signals as described in “5.1. Special Signal Definitions” on page 25, as well as for other designated signals that may be incorporated within future versions of the SERIPLEX Control Bus standard specification. This convention still allows the full 7,680-bit multiplexed data capacity.

- Multi-bit signals should be assigned on address boundaries as described in “3.3.8. Device Address Boundaries” on page 15. In particular, multiplexed signals should be assigned starting addresses that are multiples of 16.

- The signal address usage of devices should be allocated in powers of 2 for signals up to 16 bits—specifically, 1, 2, 4, 8, or 16 bits. Signals longer than 16 bits should be allocated addresses in 16-bit increments—16, 32, 48, etc. Although this allows a maximum data length of 240 bits, the recommended practice is to limit data length to 64 bits or fewer.

If more addresses are allocated to a device or signal than are actually needed to transmit that signal, the recommended practice is to assign any unused data bits the signal value of 0.

Address assignments for CDR signals are defined in “6.6.3.1. CDR Signal Address Assignments” on page 32 of this document.

There is no signal addressing convention for data echo signals.
5.3. Bit Order

Multi-bit data values can represent a binary number. Such data values will be transmitted least significant bit first—the least significant bit of the data value corresponds to the lowest address number assigned to that signal, and the most significant bit corresponds to the highest assigned signal address.

A sign bit, if used, must occupy the most significant bit within the data value.

Multi-bit discrete signals (multiple, consecutive, single-bit signals transmitted by a single device) can be transmitted in any order that is appropriate to a given device or application, although this order should remain fixed for all devices of a given type. As a general convention, input/output points should be numbered so that the lowest point number on the device corresponds to the lowest SERIPLEX address.

5.4. Data Coherence

Multi-bit values must be assigned contiguous signal address, and be entirely transmitted within a single data frame. The value of a bus signal must not change during bus transmission of that signal, regardless of that signal's length.

Any device designed to transmit or receive a multi-bit data signal must ensure that the signal is coherent—the entire signal is transmitted and received within a single data frame and is generated and used as a single unit. This requirement is specifically intended to avoid data mismatches, wherein two portions of a signal would be received as two separate objects with a change in signal value occurring between transmission of the two objects.

SERIPLEX host interfaces must ensure data coherence for signal lengths up to at least 16 bits (including CDR check information, if any).

No method of ensuring data coherence of signals longer than 16 bits is described or required by this specification. Designers and users of devices and applications that use signals and/or messages longer than 16 bits must provide their own methods to ensure data coherence as required.

6. OPERATIONAL CHARACTERISTICS

The following sections describe the operation and interaction of bus devices under various conditions.

6.1. Bus Initialization

Bus initialization and operation is controlled by a SERIPLEX system's clock source device. Although the conditions under which a clock source initiates bus operation vary among systems, they must be predictable and repeatable for the application designer in all cases.

Before initiating SERIPLEX control bus operation, a clock source must first create a clock halt condition, ensuring that the bus clock signal has been idle for at least the duration of the clock loss detect time. After the clock halt, all I/O devices assume their default signal states and are ready for normal bus initialization to begin.

The clock source begins the bus initialization process by transmitting a bus fault detection (BFD) pulse and performing the associated bus fault tests. If the clock source detects a bus fault, it transmits exactly one clock pulse, and then returns to a clock halt state, not transmitting any clock pulses for at least the duration of the clock loss detect time. This single clock pulse ensures that I/O devices do not sense enough consecutive BFD pulses on the data line to place them into programming mode (see “7. Device Programming” on page 40). Since this clock pulse corresponds to bus address 0, no bus data is transmitted during this pulse. While not recommended practice, it is acceptable for the clock source to transmit this single clock pulse before the BFD pulse instead of after, provided that the clock line has been idle for at least the duration of the clock loss detect time.
If the clock source detects no bus faults, it begins transmitting the bus clock signal and scanning data frames. Upon the first negative clock signal transition, all properly connected and powered bus devices begin their initialization processes, as described in the next section.

### 6.2. Device Initialization

All bus devices assume default bus input and output data signal states upon initial application of bus power, upon detection of bus fault or undervoltage conditions, and upon any other bus initialization condition. All bus I/O devices' external output signals assume their shelf states (typically off or deactivated) under these conditions.

On the first negative clock signal transition following a clock loss condition, bus I/O devices begin their normal process of counting clock pulses and monitoring for the sync period, for loss of the clock signal, and for bus faults.

Bus output devices can monitor bus output data, but will not change their external output signals from their default shelf state, until they have detected at least five valid sync periods and BFD pulses without loss of the clock signal. This is intended to allow bus data and device logic conditions to stabilize before actual control activity takes place, as well as to prevent improper transmission and reception of data should a device become active during the course of a data frame instead of between frames. Similarly, bus input devices will also withhold bus input signals (transmitting only signal values of 0) upon bus initialization until they have detected at least 4 valid sync periods and BFD pulses.

It is recommended practice for the bus master to withhold bus output signals (to transmit only signal values of 0) for the first 4 data frames upon bus initialization, in order to allow bus data and device logic conditions to stabilize before actual control activity takes place.

**NOTE:** The specification did not require SERIPLEX control bus version 1 I/O devices to withhold or ignore bus data for any period upon bus initialization.

"Hot plugging"—connecting a bus I/O device to a SERIPLEX bus cable while the bus is operating—is not a recommended practice.

### 6.3. Normal Bus Operation

Normal SERIPLEX control bus operation begins when all devices have completed their initialization activities and begin reporting input data and responding to output data normally. Normal bus operation typically begins with the fifth valid sync period following a clock halt condition.

During normal bus operation, the bus clock source continually generates data transmission frames by transmitting series of clock pulses separated by sync periods. Bus input devices report bus input data, bus output devices monitor and respond to bus output data, and the bus master monitors input data and reports output data, all according to their assigned signal addresses and internal logic.

If signal multiplexing is used within a given system, the clock source produces the multiplex channel indication through output signals 1 through 4, and multiplexed devices monitor this indication and respond accordingly.

All devices continually monitor for sync periods, clock loss, bus faults, and undervoltage, and respond to each of these conditions according to the requirements of this document. In addition, devices with CDR enabled transmit CDR data and monitor for CDR faults, and respond as required.

Normal bus operation ends with either the cessation of the bus clock signal or with detection of a bus fault condition. Bus devices respond to these conditions according to the requirements of this document.
6.4. Bus Fault Detection

Each I/O device on a SERIPLEX bus monitors for the presence of a bus fault detection (BFD) pulse during each sync period.

If the BFD pulse is detected and the sync period ends normally, the I/O device presumes that the bus is operating properly and allows bus output data received during the previous data frame to be transmitted to its external output signals, subject to any other fault-detection mechanisms that the device uses.

If the device fails to detect a BFD pulse during a sync period, the device recognizes a bus fault condition, and its external output signals revert to their default or shelf state immediately. The shelf state corresponds to an off or deactivated state for most bus I/O devices; the SERIPLEX ASIC2B chip turns its external output signals off upon detection of a bus fault.

Refer to “3.3.3. Bus Fault Detection Pulse” on page 13 and “4.5. Signal Timing” on page 23 for details about the bus fault detection pulse.

NOTE: The bus fault detection pulse provided by the version 1 SERIPLEX control bus clock sources was not standardized, and was implemented in several different ways. Version 1 SERIPLEX control bus I/O devices required only a positive transition of the bus data line within the sync period.

6.5. Clock-Loss Detection and Response

During operation, each SERIPLEX device (including the clock source) continually monitors the bus clock line for signal activity. If a device does not detect any clock pulses for the duration of the clock loss detect time \( t_{\text{closs}} \) (nominally 1.5 ms), that device recognizes a clock loss condition.

Upon detecting a clock loss condition, bus I/O devices assume their default (shelf) state, wherein external output signals are normally turned off. Bus I/O devices remain in their shelf states until they have completed their own initialization activities upon bus initialization.

A transition of the bus clock signal ends the clock loss condition and begins the bus initialization process. Upon detection of this first clock signal transition, devices begin their initialization processes. If the bus clock signal becomes inactive again for the duration of the clock loss detect time before initialization is completed, devices remain in their shelf states without ever beginning normal operation, and the bus initialization process must be restarted.

Upon detecting or asserting a clock loss condition, the clock source ceases transmission of bus data through the data line, and will not attempt to transmit the bus clock signal for at least the duration of the clock loss detect time. Following this period, the clock source can re-initialize the bus, as described in “6.1. Bus Initialization” on page 27.

The clock source can remain in a clock halt condition indefinitely, according to SERIPLEX bus conditions, the clock source's design, and user configuration options. The clock source can attempt to restart the bus at a maximum rate of once per clock loss detect time period.
Any time a clock source stops transmitting the bus clock signal for a period longer than the maximum sync period duration, the clock source must wait for at least the duration of the clock loss detection time before transmitting a BFD pulse or attempting to resume transmission of the bus clock signal.

**NOTE:** Clock loss is not necessarily a bus fault condition; a clock loss condition can be asserted intentionally by the bus clock source according to its design and that of the SERIPLEX control bus application.

### 6.6. Data Error Detection Methods

#### 6.6.1. Digital Signal Debounce

Digital signal debounce provides a method for a signal-receiving device to detect and filter errors in single-bit data transmissions. A device that uses digital debounce will not respond to a momentary deviation in a received signal's value. In this method, the receiving device compares a single-bit signal value received from the bus with the values received in a designated number of preceding data frames. If the data values are not identical, the device holds its corresponding internal logic signal at its last state. The device changes its internal logic state if and only if the data received from the bus remains at the new logic state for the required number of data frames.

The number of data frames for which a signal value must be identical for a device to change its logic state is called the debounce length. All bus devices must offer the ability to debounce received single-bit non-multiplexed signals for 2 or 3 data frames (debounce length = 2 or 3), as well as the ability to disable the digital debounce feature, unless such signals can be validated through CDR instead. Multi-bit and multiplexed data signals can be verified through use of the CDR feature instead of digital debounce.

**NOTE:** The SERIPLEX ASIC2B chip offers a user-selectable debounce length of 2 or 3 for each of its 2 discrete output signals.

Figure 15 depicts the state of a device's internal logic signal, given an example data stream, for debounce lengths of 2 and 3.

**Figure 15:** SERIPLEX Control Bus Digital Debounce

Upon bus initialization, each debounced signal remains in its default state at least until debounce conditions have been satisfied for that signal's change of state.

**NOTE:** The SERIPLEX ASIC2B chip disables all 3 of its discrete output signals until debounce conditions have been initially satisfied for both of its bus output signals.
6.6.2. Data Echo

Data echo provides a method for a signal-transmitting device to verify that a single-bit data signal has been received correctly by another device. This feature provides both message acknowledgment and data verification.

In this method, a device that receives a single-bit data signal retransmits that signal back to the bus. For instance, a discrete output device such as a valve could echo its control signal back onto the bus as an input signal.

The device that transmits the original signal can compare the echoed signal value to the original value to determine whether the data has been received correctly. The echoed value can be complemented (inverted) to provide additional assurance that the bus data line is not being continually driven to a logic-high or -low state.

There are no explicit requirements for the relationship between the addresses of the original signal and the echoed signal in master/slave mode. In master/slave mode, output signals and input signals are separated in time by virtue of the bus timing; therefore, it is conceivable that signals could be echoed to the same address as the original signal.

Because there is no distinction between output signals and input signals in peer-to-peer mode, a signal cannot be echoed to its same address. This would create a feedback condition that would latch the signal to a value of 1. Otherwise the same recommendations apply as for master/slave mode.

There are no explicit requirements for a transmitting device’s behavior upon detection of a data echo error; this behavior must be determined by the designers of individual applications. Note that the receiving device does not obtain data verification through this method, so the transmitting device is responsible for error detection, reporting, and response.

SERIPLEX bus devices are not required to provide a data echo feature. However, it is recommended practice for a single-bit output device to offer data echo for its primary control signal. If offering a data echo feature, the recommended practice is to offer the user the option to enable the feature, and to invert the original signal polarity before echoing the signal back to the bus.

NOTE: The SERIPLEX ASIC2B chip provides user-selectable options to echo its output A signal to its input B signal, and to echo either its output B or its output C logic signal to its input A signal.

6.6.3. Complementary Data Retransmission (CDR)

Complementary data retransmission, or CDR, is a method of verifying that a received multi-bit signal’s value matches that transmitted by the signal’s source device. This is accomplished by the source device sending an encoded version of the signal data along with the normal signal data, and the receiving device comparing the two values. If the encoded value matches the original value, the data is accepted by the receiving device; otherwise, the data is rejected.

CDR can be applied to both input and output data, in both peer-to-peer and master/slave modes. CDR can be applied to either individual bytes of data or to 16-bit words (byte pairs). CDR can be applied independently to input and output signals sharing the same address, as well as to signals sharing the same address but assigned to different multiplex channels.

All bus devices that transmit multi-bit bus input signals must provide CDR transmission capability. Bus output devices must provide CDR verification capability if they receive multi-bit numeric signals, or if they receive multi-bit, discrete signals without providing digital signal debounce capability for those signals. The recommended practice is for CDR enabling and verification to be user-selectable options for individual, multi-bit, input and/or output signals.
It is recommended practice for the enabling of a device’s CDR feature to be user-selectable. Although there are no specific requirements for the method of enabling and disabling CDR, the most common method for bus I/O devices is expected to be address assignment. For example, assigning a block of 32 addresses to a 16-bit input device would allow it to transmit its CDR check bytes, whereas assigning only 16 addresses would prevent CDR transmission.

The following sections describe the SERIPLEX bus address assignments of CDR-related signals, the CDR method of data encoding and decoding, and the responses of the bus devices to detected CDR errors.

6.6.3.1. CDR Signal Address Assignments

CDR is performed on individual bytes of input or output data. The original data bytes must be addressed on 8-bit boundaries, and must fall within a 16-bit word that is addressed on a 32-bit boundary (i.e., Address 32, 40, 64, 72, 96, 104,...). CDR cannot be designated for the data word beginning at address 0. See Table 10 for details.

<table>
<thead>
<tr>
<th>Address</th>
<th>0</th>
<th>8</th>
<th>16</th>
<th>24</th>
<th>32</th>
<th>40</th>
<th>48</th>
<th>56</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contents</td>
<td>—</td>
<td>—</td>
<td>Data 16</td>
<td>Data 24</td>
<td>Data 32</td>
<td>Data 40</td>
<td>CDR 32</td>
<td>CDR 40</td>
</tr>
<tr>
<td>Address</td>
<td>64</td>
<td>72</td>
<td>80</td>
<td>88</td>
<td>96</td>
<td>104</td>
<td>112</td>
<td>120</td>
</tr>
<tr>
<td>Contents</td>
<td>Data 64</td>
<td>Data 72</td>
<td>CDR 64</td>
<td>CDR 72</td>
<td>Data 96</td>
<td>Data 104</td>
<td>CDR 96</td>
<td>CDR 104</td>
</tr>
<tr>
<td>Address</td>
<td>128</td>
<td>136</td>
<td>144</td>
<td>152</td>
<td>160</td>
<td>168</td>
<td>176</td>
<td>184</td>
</tr>
<tr>
<td>Contents</td>
<td>Data 128</td>
<td>Data 136</td>
<td>CDR 128</td>
<td>CDR 136</td>
<td>Data 160</td>
<td>Data 168</td>
<td>CDR 160</td>
<td>CDR 168</td>
</tr>
<tr>
<td>Address</td>
<td>192</td>
<td>200</td>
<td>208</td>
<td>216</td>
<td>224</td>
<td>232</td>
<td>240</td>
<td>248</td>
</tr>
<tr>
<td>Contents</td>
<td>Data 192</td>
<td>Data 200</td>
<td>CDR 192</td>
<td>CDR 200</td>
<td>Data 224</td>
<td>Data 232</td>
<td>CDR 224</td>
<td>CDR 232</td>
</tr>
</tbody>
</table>

Each data byte’s corresponding CDR check value is transmitted 16 addresses following the original data value. For instance, the CDR check value for the data byte at addresses 32-39 is transmitted at addresses 48-55.

In systems where CDR is enabled for any data word, the clock source broadcasts the logical inverse (the complement of 1) of the multiplex channel indication bits (outputs 1 through 4) at outputs 5 through 8. Each bit’s complement is transmitted 4 addresses after the original bit.

CDR-enabled bus output devices can use input 9 to indicate detection of a CDR data error. Since all output devices share this indication method, it is possible that multiple output devices could simultaneously detect and report CDR errors through this method. This document does not specify any method for determining which output device is reporting a CDR error.

It is permissible to treat two adjacent data bytes as a single, 16-bit data value for the purpose of CDR evaluation. In this case, an error detected in either byte would cause the receiving device to reject the entire word.

The recommended practice is for host controllers to provide the user with the choice to have adjacent input data bytes evaluated separately, or as a single, coherent data word. Output bytes can also be combined similarly, if it is appropriate for the specific output device being used, such as with a 16-bit analog signal.
It is acceptable to use individual data bytes for normal data transmission without restriction, when CDR is not enabled. Likewise, the corresponding CDR bytes are also permitted for use in normal data transmission, when CDR is not enabled.

6.6.3.2. CDR Data Encoding

In addition to verifying the value of a data signal, CDR data encoding verifies the identity of a data signal, including the signal's complete address as well as the data itself. This is accomplished by encoding the data with values indicating the signal's address, multiplex channel, and direction (input vs. output), according to the following formula:

\[ c = d \oplus e \]

where:

- \( c \) = CDR check byte
- \( d \) = original data byte
- \( e \) = encoding byte
- \( \oplus \) represents a bitwise exclusive-OR logic function

The original data can be recovered from the encoded data by applying the converse formula:

\[ d = c \oplus e \]

The encoding byte is formed by concatenating four-bit codes representing a signal's assigned address and multiplex channel, with the multiplex channel code also modified according to whether the signal represents input or output data, according to the following formula:

\[ e = a \| (m' \oplus io) \]

where:

- \( e \) = encoding byte
- \( a \) = address code (four bits)
- \( m' \) = multiplex channel code (four bits)
- \( io \) = input vs. output code (four bits)
- \( \| \) denotes a concatenation operation, with “a” occupying the four most significant bits of the encoding byte, and “m' \oplus io” the least significant bits.

Table 11 lists the four-bit address codes (a). These address codes ensure that encoding inverts at least one bit of the original data and leaves at least one bit non-inverted.

<table>
<thead>
<tr>
<th>Starting Address</th>
<th>Address Code (a)</th>
<th>Starting Address</th>
<th>Address Code (a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>0001</td>
<td>136</td>
<td>1000</td>
</tr>
<tr>
<td>40</td>
<td>0010</td>
<td>160</td>
<td>1001</td>
</tr>
<tr>
<td>64</td>
<td>0011</td>
<td>168</td>
<td>1010</td>
</tr>
<tr>
<td>72</td>
<td>0100</td>
<td>192</td>
<td>1011</td>
</tr>
<tr>
<td>96</td>
<td>0101</td>
<td>200</td>
<td>1100</td>
</tr>
<tr>
<td>104</td>
<td>0110</td>
<td>224</td>
<td>1101</td>
</tr>
<tr>
<td>128</td>
<td>0111</td>
<td>232</td>
<td>1110</td>
</tr>
</tbody>
</table>

The right-most digit represents the least significant bit of the code. Data is transmitted through the SERIPLEX bus with least significant bit first.
Table 12 lists the four-bit multiplex channel codes (m'). The designation m' is used to indicate that the multiplex channel code represents the logical inversion (the complement of 1) of the multiplex channel indication broadcast by the bus clock source. Again, the right-most digit represents the least significant bit of the code.

**Table 12: Channel Codes**

<table>
<thead>
<tr>
<th>MUX Channel</th>
<th>MUX Code (m')</th>
<th>MUX Channel</th>
<th>MUX Code (m')</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1111</td>
<td>8</td>
<td>0111</td>
</tr>
<tr>
<td>1</td>
<td>1110</td>
<td>9</td>
<td>0110</td>
</tr>
<tr>
<td>2</td>
<td>1101</td>
<td>10</td>
<td>0101</td>
</tr>
<tr>
<td>3</td>
<td>1100</td>
<td>11</td>
<td>0100</td>
</tr>
<tr>
<td>4</td>
<td>1011</td>
<td>12</td>
<td>0011</td>
</tr>
<tr>
<td>5</td>
<td>1010</td>
<td>13</td>
<td>0010</td>
</tr>
<tr>
<td>6</td>
<td>1001</td>
<td>14</td>
<td>0001</td>
</tr>
<tr>
<td>7</td>
<td>1000</td>
<td>15</td>
<td>0000</td>
</tr>
</tbody>
</table>

The right-most digit represents the least significant bit of the code. Data is transmitted through the SERIPLEX bus with least significant bit first.

Table 13 lists the four-bit I/O direction codes. These codes are selected to invert the most significant bit of the multiplex channel code (m') if and only if the data represents master/slave mode output data. As before, the right-most digit corresponds to the least significant bit of the code.

**Table 13: I/O Direction Codes**

<table>
<thead>
<tr>
<th>SERIPLEX Control Bus Operating Mode</th>
<th>Data Transmission Direction</th>
<th>I/O Direction Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peer-to-peer Inputs</td>
<td>Inputs</td>
<td>0000</td>
</tr>
<tr>
<td>Peer-to-peer Outputs</td>
<td>Outputs</td>
<td>0000</td>
</tr>
<tr>
<td>Master/slave Inputs</td>
<td>Inputs</td>
<td>0000</td>
</tr>
<tr>
<td>Master/slave Outputs</td>
<td>Outputs</td>
<td>1000</td>
</tr>
</tbody>
</table>

The right-most digit represents the least significant bit of the code. Data is transmitted through the SERIPLEX bus with least significant bit first.

For example, if the original data byte were decimal 163 (binary 10100011), to be transmitted as master/slave mode output data at address 32 during multiplex channel 3, the corresponding check byte would be formed as shown in Figure 16.

Data Byte (d) → \[1010 \ 0011\] = Decimal 163

Address Code (a) → \[0001 \ 1100\] ← Multiplex Channel Code (m')

\[1000\] ← I/O Direction Code (io)

Check Byte (c) → \[1011 \ 0111\] = Decimal 183

**Figure 16: Check Byte Formation**
6.6.3.3. CDR Error Response

A CDR error is defined as a mismatch between the value of a data byte and the value of its corresponding CDR check byte. Since CDR is verified by the signal-receiving device, output CDR errors are detected by bus output devices, and input CDR errors are detected by a bus master device.

In practice, input CDR errors are detected by a clock source device, a host interface, a host controller, or a control software application executed by a host controller. For the purpose of this discussion, these devices are collectively referred to as a "bus master device".

**Output CDR errors:** Upon detection of an output CDR error, a bus output device rejects the associated output data. At this point, the output device either declares an output CDR fault immediately, or it rides through (continues to operate normally) for three signal updates. In the latter case, the output device retains its last valid output signal value until either a new valid value is received through the bus, or until the third consecutive invalid transmission is received. Once this ride-through limit is reached, the output device declares an output CDR fault.

When an output device declares an output CDR fault, it sets the output signal values to their default states. The device also sets the SERIPLEX bus input 9 signal to 1, to indicate to other devices that the device has declared an output CDR fault. This indication method, however, does not identify the individual signal or device that experienced the fault—any such identification must be performed by the control application.

Each output device provides a single fault indication for all of its output signals. The device also combines the ride-through count for the output signals, so errors detected in different output signals will all count towards a single ride-through limit.

The ride-through count is incremented no more than once per data frame, even if an output device detects CDR errors in both the multiplex channel indication and an output signal, or for more than one output signal.

The output device clears output CDR errors and faults when all of the output signals in a single frame of output data are received without CDR errors. Then the device accepts the frame’s signal data for use by the device’s external circuitry. The output device also stops asserting the output CDR fault indication, and the ride-through count is cleared to 0. Output CDR error conditions are also cleared when the output device is re-initialized.

Bus masters and other bus devices can respond to the output CDR fault at input 9 in any manner that is appropriate for the application. However, if the master device is a host interface, the interface unit must provide a means to inform the host controller of the output CDR fault condition. The recommended practice is for master devices to offer the user the choice of halting the SERIPLEX bus or ignoring the output CDR fault message.

Bus output devices that provide CDR capability must provide either immediate declaration of a CDR fault, ride-through capability, or both. The recommended practice is to make the response method user-selectable. Either immediate fault declaration or ride-through can be used as a default setting.

**Input CDR errors:** Upon detection of an input CDR error, a bus master device rejects the associated input data. At this point, the master device either declares an input CDR fault immediately, or it rides through (continues to operate normally) for three signal updates. In the latter case, the bus master device retains its last valid input signal value until either a new valid
value is received through the bus, or until the third consecutive invalid transmissions is received. Once the ride-through limit is reached, the master device declares an input CDR fault.

When a master device declares an input CDR fault, it sets the value of the affected input data signal to 0. At this point, the device may also halt the SERIPLEX bus (ceasing transmission of the bus clock signal). If the master device is a host interface, the interface unit must provide a means to inform the host controller of the input CDR fault condition.

A bus master device can either identify a unique input CDR fault for each individual input signal or use a single fault indication for a designated group of input signals. However, the device must still clear data and keep a ride-through count for individual signals, so a CDR error for one input signal will not affect the data value or ride-through count of another input signal.

The ride-through count is incremented no more than once per data frame, even if a device detects CDR errors in both the multiplex channel indication and an input signal.

An input CDR error condition for a given input signal is cleared upon detection of a single, valid transmission of that signal. At the time valid data is received, the master device clears the signal's ride-through count to 0 and accepts the signal data for use by the host application. Input CDR error conditions are also cleared when the master device is re-initialized.

Bus master devices must provide either immediate declaration of an input CDR fault, ride-through capability, or both. The recommended practice is to make the response method user-selectable. Either immediate fault declaration or ride-through can be used as a default setting.

Bus master devices must provide the capability to halt the SERIPLEX bus upon declaration of an input CDR fault. The recommended practice is to offer the user the choice of ignoring input CDR faults (reporting the fault condition and clearing the input data, but continuing to operate the bus). If the choice is offered, the default selection must be to halt the bus.

The following sections define fault conditions that can be detected by SERIPLEX bus I/O devices. Each section defines the fault and specifies requirements for fault detection and response.

6.7. Faults and Responses

6.7.1. I/O Device Faults and Responses

The default state of bus output devices is the vendor-determined state that the device's external output signals assume upon detecting a fault condition. Typically, the default state of a device output corresponds to a signal value of 0. However, it is permissible for the default state of the device to be any value designated as appropriate by the device vendor, or for the defaults to be user-selectable. For example, an analog output device might provide user-selectable default states of zero, half scale, full scale, or last state.

The shelf state of bus output devices is the vendor-determined state that the device's external output signals assume upon loss of logic power. Typically, the shelf state of a device output is designated as inactive, and corresponds to a signal value of 0. However, device vendors can specify other shelf states, as appropriate for a given type of device. The recommended practice is that the default state and shelf state of a device are the same, unless a different default state is intentionally selected by the device user.

NOTE: The SERIPLEX ASIC2B chip disables its external output signals (asserting a signal value of 0) upon detection of a bus fault, undervoltage, or clock loss condition.
6.7.1.1. Bus Fault

All SERIPLEX bus I/O devices must monitor for bus fault conditions, as defined in “6.4. Bus Fault Detection” on page 29. Upon detecting a bus fault condition, an I/O device’s external output signals will revert to their default states.

Once it has detected a bus fault condition, an I/O device must be re-initialized before it will resume normal operation. The I/O device’s signals will remain in their default states until all bus and I/O device initialization procedures have been completed upon bus re-initialization.

6.7.1.2. Power Loss and Undervoltage

Each bus I/O device within a SERIPLEX system will monitor for bus voltage below the specified minimum operating voltage. Upon detection of an undervoltage condition of the bus power line, an I/O device’s external output signals will revert to their shelf states.

Once normal power has been restored to an I/O device following an undervoltage condition, the device must be re-initialized before it will resume normal operation. The I/O device’s signals will remain in their shelf states until all bus and I/O device initialization procedures have been completed upon bus re-initialization.

6.7.1.3. CDR Errors

Bus output devices can monitor for output CDR errors, as defined in “6.6.3. Complementary Data Retransmission (CDR)” on page 31.

6.7.1.4. Data Echo Error

A data echo error is typically a mismatch between a data signal and its echoed value, as defined in “6.6. Data Error Detection Methods” on page 30. This document does not specify any requirements for a device’s response upon detection of a data echo error; this response can be defined by an application designer as appropriate.

In most cases, data echo is evaluated by a controller rather than an I/O device.

6.7.1.5. I/O Device Fault

It is permissible to have a SERIPLEX control bus I/O device respond to fault conditions internal to that device in any manner deemed appropriate by the designer of that device and the designer of the application in which the device is installed.

It is recommended practice for I/O devices not to interfere with operation of the control bus to the extent possible under device fault conditions. It is also recommended practice for I/O devices’ signals to assume their shelf states upon detection of an internal device fault, to remain in this state until the internal fault has been cleared, and to require complete device reinitialization before resuming normal operation.

6.7.2. Clock Source Faults and Responses

The following sections define fault conditions that can be detected by SERIPLEX bus clock sources. Each section defines the fault and specifies requirements for fault detection and response.
It is recommended practice that clock sources be able to withstand any listed bus fault without incurring physical or permanent damage.

It should be made clear both to SERIPLEX device designers and to application designers that the clock source cannot directly detect the presence of bus faults at remote locations. For instance, a clock source may not be able to detect the presence of a short between the bus data and power lines through 3,000 feet of bus cable, due to the resistance and voltage drop through the cable. Other methods must be used to detect fault conditions such as excess capacitance at locations remote from the clock source.

6.7.2.1. General Clock Source Response

Except where specifically noted, the clock source will cease transmission of the bus clock signal immediately upon detection of any of the SERIPLEX bus fault conditions listed below. This effectively halts transmission of bus data.

Upon initial detection of a fault during a sync period when the bus has been operating normally, the clock source will not transmit a clock pulse at the end of that sync period, and will not transmit any clock pulses for at least the duration of the clock loss detect time.

Once the clock loss detect time has elapsed without transmission of any clock pulses, the clock source can attempt to restart the bus, according to “6.1. Bus Initialization” on page 27.

6.7.2.2. Data Line Faults

All SERIPLEX clock sources will monitor the bus data line to determine whether it is possible to drive the data line to both logic-high and -low states. This test will be performed during each sync period through the transmission and reception of the BFD pulse, in accordance with the requirements of “3.3.3. Bus Fault Detection Pulse” on page 13 and “6.3. Normal Bus Operation” on page 28.

If the clock source is not able to drive the bus data line to both logic-high and -low states, it recognizes a data line fault condition. Data line faults include both data stuck high and data stuck low conditions.

The clock source can indicate the data line fault condition to a user or to a host controller by any means deemed appropriate by the clock source designer and application designers.

6.7.2.3. Clock Line Faults

All SERIPLEX clock sources will continually monitor the bus clock line to determine whether the clock line is changing logic states in accordance with the clock source’s commands. If the logic state of the clock line ever fails to match the commanded state (with allowance made for capacitive signal delays), the clock source will recognize a clock fault condition. Clock fault conditions include clock stuck high, clock stuck low, and clock loss.

The clock source can indicate the clock fault condition to a user or to a host controller by any means deemed appropriate by the clock source designer and application designers.
6.7.2.4. Clock-to-Data Short

All SERIPLEX clock sources will continually monitor for the presence of electrical shorts between the SERIPLEX clock and data lines. A test for this condition will be performed at least once per data frame.

The exact method for detecting this fault is not specified within this document. However, one possible method is to measure data line current during the BFD pulse, to detect the excess current that would be fed from the clock line to the data line during a short condition.

The clock source can indicate the clock-to-data short condition to a user or to a host controller by any means deemed appropriate by the clock source designer and application designers.

6.7.2.5. Excess Data Line Capacitance

All SERIPLEX clock sources will continually monitor for excess capacitance on the SERIPLEX bus data line. This test is intended to detect when the bus data line fails to recharge fast enough to prevent false data readings (see “4.2. Data Line Characteristics” on page 18). This effect usually results from operating the bus at a clock rate that is too fast for the amount of bus cable and/or quantity of I/O devices in the system.

The excess capacitance test will be performed during each sync period by testing the logic status of the bus data line one-half clock period after the positive transition of the BFD pulse. If the measured data line voltage is not greater than the logic-high threshold (7.5 Vdc) by this time, the clock source recognizes an excess capacitance fault.

The clock source can indicate the excess capacitance fault to a user or to a host controller by any means deemed appropriate by the clock source designer and application designers.

6.7.2.6. Power Loss and Undervoltage

All SERIPLEX clock sources will continually monitor the bus power voltage to determine whether it is above the specified minimum voltage. If this voltage is not present or is below the specified minimum, the clock source recognizes an undervoltage condition.

The clock source can indicate the undervoltage fault condition to a user or to a host controller by any means deemed appropriate by the clock source designer and application designers.

6.7.2.7. Other Bus Faults

This document makes no explicit requirements for other types of bus faults that a clock source can detect. However, the types of faults that a clock source detects and the clock source’s responses to those faults must be predictable to an application designer who uses that clock source.

Other types of SERIPLEX bus faults that might be detected by a clock source include data line overcurrent and undercurrent.

It is recommended practice for the bus clock source to cease transmitting bus clock and data signals upon recognition of any bus fault condition. However, it is acceptable for clock source designers to provide a user-selectable override feature to allow the clock source to continue normal bus operation in the presence of any optional bus fault.
6.7.2.8. Internal Faults

This document makes no explicit requirements for types of internal clock source faults that a clock source detects. However, the types of faults that a clock source detects and the clock source’s responses to those faults must be predictable to an application designer making use of that clock source.

The types of internal faults that might be detected by a clock source include internal RAM failure, internal watchdog fault, and host watchdog fault.

It is recommended practice for the bus clock source to cease transmitting bus clock and data signals upon recognition of any internal fault condition. However, it is acceptable for clock source designers to provide a user-selectable override feature that would allow the clock source to continue bus operation in the presence of some types of internal clock source faults.

6.7.2.9. CDR Errors

Clock source devices must be capable of monitoring for input and output CDR errors, as defined in “6.6.3. Complementary Data Retransmission (CDR)” on page 31.

6.7.2.10. Data Echo Error

A data echo error is typically a mismatch between a data signal and its echoed value, as defined in “6.6. Data Error Detection Methods” on page 30. Typically application logic within a host controller detects and responds to this error. It is conceivable that data echo errors could be detected by a clock source such as a host interface device, but this document does not specify any means by which original and echoed signal addresses and polarities are matched.

This document does not specify any requirements for a host's response upon detection of a data echo error; the application designer is permitted to define this response as appropriate.

7. DEVICE PROGRAMMING

Programming or configuration of a bus I/O device through that device’s SERIPLEX bus connection port is performed according to the methods described in the SERIPLEX Technology Organization’s SERIPLEX ASIC2B Data Sheet (8310PD9601).

The operation of the SERIPLEX clock source, bus I/O devices, the bus power supply, and or the bus itself must not unintentionally place I/O devices into their programming mode, nor write configuration data into I/O devices.

Programming of multiple bus I/O devices simultaneously through the same SERIPLEX cable is not a recommended practice, nor is attempting to program a single bus I/O device while other devices are connected to the same SERIPLEX cable.

There are no requirements, restrictions, or conventions for programming of bus I/O devices by methods other than through their SERIPLEX bus connection ports.

During programming of devices containing the ASIC2B chip, during which all external input and output signals are disabled, I/O devices must not draw more than 100 mA from the bus power line. I/O devices that do not incorporate the SERIPLEX ASIC2B chip and that, therefore, must use a different method of device configuration than that of the ASIC2B chip, are exempt from this requirement.
The programming sequence will begin at least 100 ms following stabilization of the bus power voltage. By this time the device must complete any power-on reset checks and any other necessary processing.

For reference only, some significant aspects of programming I/O devices that incorporate the SERIPLEX ASIC2B chip are listed below:

- To place the ASIC2B chip into its programming mode, the ASIC power must be within the range of 15 to 16.5 Vdc, the clock signal must remain idle for at least 40.5 ms, and the ASIC2B chip must detect 15 positive transitions of the data signal while the clock signal is held at the logic-high state following the 40.5 ms waiting period.
- Once the ASIC2B chip is in the programming mode, the state of the data line upon the first negative transition of the clock signal determines whether an ASIC2B data read or write operation will be performed.
- ASIC2B configuration data is shifted into or out of the ASIC2B chip's EEPROM memory through the bus clock and data lines.
- If the EEPROM write data has been successfully received by the ASIC2B chip, the chip asserts a busy signal by holding the data line low until the EEPROM writing operation is complete.

8. SIGNAL RESPONSE TIME

The following information is provided for reference only, to demonstrate the methods of calculating signal update and response times within a control bus system. These update and response times are dependent upon a variety of factors including bus frame length, clock rate, clock source sync period duration, and I/O device propagation delays. These response time calculations do not represent specifications for the performance of SERIPLEX control bus systems.

8.1. Frame Period (t_F)

A frame period is defined as the elapsed time between the end of successive sync periods while a SERIPLEX bus system is operating normally. Within a given system, the frame period is fixed, and is determined by the designated frame length, clock rate, and sync period (t_sync):

\[ t_F = \frac{(mode \times \text{frame length}) + 8}{\text{clock rate}} \]

where mode = 1 for peer-to-peer operation and mode = 2 for master/slave operation.

For clock rates above 100 kHz, the sync period is normally 16 clock periods in duration, so the frame period is calculated as:

\[ t_F = \frac{(mode \times \text{frame length}) + 16}{\text{clock rate}} \]

As the formulae indicate, the frame period can be reduced either by shortening the frame length or by increasing the clock rate.

8.2. Signal Update Time (t_U)

Signal update time is defined as the elapsed time between successive transmissions of a particular signal through the SERIPLEX bus—in other words, how often an individual signal value is reported through the SERIPLEX bus. The longest signal update time for any signal within a given system also defines the time required to update all the bus data within that system.
For non-multiplexed signals, the signal update time equals the frame period:

\[ t_U = t_F \]

For multiplexed signals, the signal update time usually equals the frame period times the number of multiplex channels scanned by the clock source \((N_{ch})\):

\[ t_U = t_F \times N_{ch} \]

If a multiplexed priority channel is designated, the calculations are modified as follows:

**Priority Channel:**

\[ t_U = t_F \times 2 \]

**Non-Priority Channels**

\[ t_U = t_F \times 2 \times (N_{ch} - 1) \]

for typical version 2 clock sources

\[ t_U = t_F \times 2 \times N_{ch} \]

for typical version 1 clock sources

### 8.3. Input Response Time \((t_{IR})\)

In **peer-to-peer mode**, input response time is defined as the elapsed time between an external input signal event and that signal's appearance on the SERIPLEX bus.

Since the timing of the input event is probably not synchronized with the operation of the SERIPLEX bus, the maximum input response time for a given signal is primarily determined by the signal update time. The propagation delay \((t_{ip})\) of the input device also affects the input response time, although this factor is usually negligible compared to the signal update time:

\[ t_{IR} = t_U + t_{ip} \]

This formula holds true for both multiplexed and non-multiplexed signals.

In **master/slave mode**, input response time is defined as the elapsed time between an external input signal event and that signal's availability to a host controller's internal logic processor. In the case of a typical backplane interface, this would be the time from the input event until new input data is posted in the interface's dual-port memory for use by application software.

Master/slave input response time is determined by the propagation delay \((t_{ip})\) of the input device, the signal update time \((t_U)\), the propagation delay \((t_{hip})\) of the host interface, and whether input data is posted immediately when received or withheld until completion of bus fault detection (BFD) checks.

The input response time formula for **immediately-posted data** is:

\[ t_{IR} = t_{ip} + t_U + t_{hip} \]

Since input propagation delay can usually be disregarded, and the host propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for input response time is usually performed as follows:

\[ t_{IR} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32]/\text{clock rate} \]

**NOTE:** For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value. Consult the interface vendors' specifications.
For non-multiplexed systems, \( N_{ch} = 1 \)

If data posting is witheld until BFD checks are completed, an extra delay \( (t_{eof}) \) from the time the signal is reported on the SERIPLEX bus until the end of the following sync period is introduced. This end-of-frame delay is determined by the frame length and the signal’s address \( (input_addr) \):

\[
t_{eof} = \frac{[(2 \times \text{frame length} + 8) - (2 \times \text{input_addr})]}{\text{clock rate}}
\]

Therefore the complete input response time formula becomes:

\[
t_{IR} = t_{ip} + t_{U} + t_{hip} + t_{eof}
\]

Under the assumptions given above, this would be calculated as:

\[
t_{IR} = \frac{[(2 \times \text{frame length} + 8) \times \text{N}_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{input_addr})]}{\text{clock rate}}
\]

which can be simplified to:

\[
t_{IR} = \frac{[(2 \times \text{frame length} + 8) + (\text{N}_{ch} + 1) + 32 - (2 \times \text{input_addr})]}{\text{clock rate}}
\]

NOTE: For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value. Consult the interface vendors’ specifications.

For non-multiplexed systems, \( N_{ch} = 1 \)

If the digital debounce feature of SERIPLEX version 2 interface cards is used, input response time can still be calculated by the same formula. In this case, the selected number of data samples \( (2 \text{ or } 3) \) should be substituted for the number of multiplex channels \( (N_{ch}) \). Digital debounce and address multiplexing cannot be used simultaneously for the same signal.

### 8.4. Output Response Time \( (t_{OR}) \)

In **peer-to-peer mode**, output response time is defined as the elapsed time between a signal’s appearance on the SERIPLEX bus and the corresponding change in state of a bus output device’s external output signal.

Since SERIPLEX bus output devices hold output data until a valid BFD check is made before passing the data on to the physical outputs, the primary component of peer-to-peer output response time is the end-of-frame delay \( (t_{eof}) \) from the time the signal is reported on the SERIPLEX bus until the end of the following sync period. The propagation delay \( (t_{op}) \) of the output device also affects the output response time, although this factor is usually negligible as compared to the end-of-frame delay:

\[
t_{OR} = t_{eof} + t_{op}
\]

where:

\[
t_{eof} = \frac{(\text{frame length} + 8 - \text{output_addr})}{\text{clock rate}}
\]

NOTE: For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value. Consult the interface vendors’ specifications.

This formula holds true for both multiplexed and non-multiplexed signals.
If the digital debounce feature of SERIPLEX version 2 output devices is used, output response time becomes:

\[ t_{OR} = t_{eof} + t_{op} + (\text{deb}_l\text{gth} \times t_U) \]

where \( \text{deb}_l\text{gth} \) is the selected debounce length for the signal—the number of identical data samples (2 or 3) required before the corresponding output changes state. Digital debounce and address multiplexing cannot be used simultaneously for the same signal.

In **master/slave mode**, output response time is defined as the elapsed time between a signal’s assertion by the host controller’s internal logic processor (usually into a backplane interface’s dual-port memory) and the corresponding change in state of an external output signal.

Since the writing of output data into a backplane interface’s dual-port memory is not synchronized with the operation of the SERIPLEX bus, the maximum output response time for a given signal is primarily determined by the signal update time. There is also an end-of-frame delay \( t_{eof} \) as described for peer-to-peer output response time. Finally, the propagation delays of both the host interface \( t_{hop} \) and the output device itself \( t_{op} \) contribute to the total output response time.

The complete output response time formula is:

\[ t_{OR} = t_{U} + t_{hop} + t_{eof} + t_{op} \]

Since output propagation delay can usually be disregarded, and the host propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for output response time is usually performed as follows:

\[ t_{OR} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{output_addr})]/\text{clock rate} \]

which can be simplified to:

\[ t_{OR} = [(2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 32 - (2 \times \text{output_addr})]/\text{clock rate} \]

**NOTE:** For clock rates greater than 100 kHz, the factor of 8 in the above formula can change to 16 or to some other value. Consult the interface vendors’ specifications.

For non-multiplexed systems, \( N_{ch} = 1 \)

If the digital debounce feature of SERIPLEX version 2 discrete output devices is used, output response time can still be calculated by the same formula. In this case, the debounce length \( \text{deb}_l\text{gth} \) of 2 or 3 data samples should be substituted for the number of multiplexed channels \( N_{ch} \). Digital debounce and address multiplexing cannot be used simultaneously on the same signal.

**8.5. System Response Time \( t_{SR} \)**

SERIPLEX bus system response time is defined as the elapsed time between an external input signal event and a resulting change in state of an external output signal.

For the SERIPLEX bus **peer-to-peer mode**, system response time is simply the sum of input response time and output response time:

\[ t_{SR} = t_{IR} + t_{OR} \]

More completely, this formula becomes:

\[ t_{SR} = t_{ip} + t_{U} + t_{eof} + t_{op} \]
Disregarding input and output propagation delays as before, this formula is typically calculated as:

\[ t_{SR} = \frac{[(\text{frame length} + 8) \cdot N_{\text{ch}} + (\text{frame length} + 8) - \text{output_addr}]}{\text{clock rate}} \]

which can be simplified to:

\[ t_{SR} = \frac{[(\text{frame length} + 8) \cdot (N_{\text{ch}} + 1) - \text{output_addr}]}{\text{clock rate}} \]

**NOTE:** For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value. Consult the clock source vendors’ specifications.

For non-multiplexed systems, \( N_{\text{ch}} = 1 \)

If the digital debounce feature of SERIPLEX version 2 discrete output devices and interface cards is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (\( N_{\text{ch}} \)). Digital debounce and address multiplexing cannot be used simultaneously on the same signal.

For SERIPLEX **master/slave mode** systems, system response time factors include host controller processing time \( t_{HR} \) as well as input response time \( t_{IR} \) and output response time \( t_{OR} \):

\[ t_{SR} = t_{IR} + t_{HR} + t_{OR} \]

Disregarding input and output propagation delays, this formula is typically calculated as:

\[ t_{SR} = \frac{[2 \cdot [(2 \cdot \text{frame length} + 8) \cdot (N_{\text{ch}} + 1) + 64 - (2 \cdot \text{input_addr}) - (2 \cdot \text{output_addr})]}{\text{clock rate}} + t_{HR} \]

If the digital debounce feature is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (\( N_{\text{ch}} \)). Digital debounce and address multiplexing cannot be used simultaneously on the same signal.

Host controller processing time is beyond the control of SERIPLEX bus devices, and is dependent on a wide variety of factors including processor type and speed, control program type and size, and data polling methods.

### 9. BUS CABLE AND CONNECTOR SPECIFICATIONS

This section lists characteristics of methods and devices used to physically connect SERIPLEX devices and to convey bus signals within a SERIPLEX system.

All cables consist of either four or six power and/or signal conductors, each insulated with high-density foam-polyethylene (HDPE). Additionally, each cable contains an aluminum/polyester foil shield and either a 22 AWG drain wire or braid shield. All cables are jacketed overall with either orange polyvinyl chloride (PVC) or black polyethylene (for direct-burial cables).

The four primary SERIPLEX control bus conductors (power, common, data, clock) and the drain wire are contained within the shield. The cable lay-up is a 4.00” (101.6 mm) left-hand lay with the following order: power, data, common, clock. This lay-up order reduces coupling between the data and clock conductors. In the case of six-conductor cables, the two additional conductors (I/O+ and I/O-) are located outside the shield but within the outer jacket. Refer to Figures 17 and 18 on page 47.
All constituent wires are stranded, with the characteristics in Table 14. Each strand is tin-coated soft annealed copper per ASTM B-33, latest issue.

**Table 14: Wire Size and Characteristics**

<table>
<thead>
<tr>
<th>AWG Wire Size</th>
<th>Construction</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>7 strands x 30 AWG</td>
</tr>
<tr>
<td>18</td>
<td>16 strands x 30 AWG</td>
</tr>
<tr>
<td>16</td>
<td>26 strands x 30 AWG</td>
</tr>
<tr>
<td>14</td>
<td>19 strands x 27 AWG</td>
</tr>
<tr>
<td>12</td>
<td>65 strands x 30 AWG</td>
</tr>
</tbody>
</table>

General electrical characteristics common to all SERIPLEX control bus cables are as shown in Table 15.

**Table 15: General SERIPLEX Cable Characteristics**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>75 °C</td>
</tr>
<tr>
<td>Working voltage</td>
<td>300 V</td>
</tr>
<tr>
<td>Dielectric strength (primary conductors)</td>
<td>5000 VDC</td>
</tr>
<tr>
<td>Dielectric strength (I/O+ and I/O− conductors)</td>
<td>1500 VDC</td>
</tr>
</tbody>
</table>

Grounded capacitance is specified for each of the two signal conductors (data, clock), and is measured for each individual conductor with respect to all other conductors (i.e., with all other conductors shorted together).

Table 16 lists complete cable parameters. Figures 17 and 18 illustrate the SERIPLEX control bus cable.

**Table 16: SERIPLEX Control Bus Cable Specifications**

<table>
<thead>
<tr>
<th>Cable Part No., O. D. (nominal), Shield &amp; Drain, 1st Pair Size, 2nd Pair Size, 3rd Pair Size, Grounded Capacitance (2nd pair), Rated, Cable Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBL1622P16 0.360 in. (9.14 mm) Foil with 22 AWG 16 AWG 22 AWG n/a 16 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBL1622P16BS 0.375 in. (9.52 mm) Foil and braid 16 AWG 22 AWG n/a 16 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBL1622P16DB 0.360 in. (9.14 mm) Foil with 22 AWG 16 AWG 22 AWG n/a 16 pF/ft. ±10% CL2 Direct burial jacket</td>
</tr>
<tr>
<td>CBL162212P16 0.472 x 0.351 in. (0.9 x 8.92 mm) Foil with 22 AWG 16 AWG 22 AWG 12 AWG 16 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBL162214P16 0.454 x 0.351 in. (11.5 x 8.92 mm) Foil with 22 AWG 16 AWG 22 AWG 14 AWG 16 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBL162216P16 0.443 x 0.351 in. (11.2 x 8.92 mm) Foil with 22 AWG 16 AWG 22 AWG 16 AWG 16 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBL1822P20 0.300 in. (7.62 mm) Foil with 22 AWG 18 AWG 22 AWG n/a 20 pF/ft. ±10% CL2</td>
</tr>
<tr>
<td>CBLFEP1622P16 0.310 in. (7.87 mm) Foil with 22 AWG 16 AWG 22 AWG n/a 16 pF/ft. ±10% CL2P Teflon coated</td>
</tr>
<tr>
<td>CBLFEP162212P16 0.420 x 0.310 in. (10.67 x 7.87 mm) Foil with 22 AWG 16 AWG 22 AWG 12 AWG 16 pF/ft. ±10% CL2P Teflon coated</td>
</tr>
</tbody>
</table>

1. Characteristic impedance of the cables listed is 85 Ω, ±10 Ω @ 10 kHz to 10 MHz.
2. Propagation velocity for all of the cables listed is 78% nominal, with a tolerance of ±10%.
9.2. SERIPLEX Connectors

The mini- and micro-style, quick-change connectors and tee-junction connectors used in a SERIPLEX system must comply with the following standards:

- ANSI/B93.55M-1981 mini standard
- SAE H1738-2 specification for mini-, micro-, and nano-style plugs and receptacles

Tables 17, 18, and 19 further list the required characteristics of any connector used in a SERIPLEX system.

**Table 17: Physical Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupling nut material</td>
<td>anodized, machined aluminum or die-case Zamak #5, with bright zinc plate and clear chromate sealer, or with epoxy coating</td>
</tr>
<tr>
<td>Contact material</td>
<td>copper alloy</td>
</tr>
<tr>
<td>Contact plating</td>
<td>30 ( \mu ) inch gold over 50 ( \mu ) inch nickel</td>
</tr>
<tr>
<td>Molded head material</td>
<td>PVC (orange)</td>
</tr>
<tr>
<td>Insert material</td>
<td>PVC (orange)</td>
</tr>
<tr>
<td>Vibration</td>
<td>2,000,000 cycles per SAE (#H1738-2)</td>
</tr>
<tr>
<td>Cable strain relief</td>
<td>30-lb. minimum, per UL 817</td>
</tr>
</tbody>
</table>
Table 18: Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage rating</td>
<td>300 V</td>
</tr>
<tr>
<td>Current rating</td>
<td>3 A</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>&lt;5 mΩ</td>
</tr>
<tr>
<td>Isolation resistance</td>
<td>&gt;100 MΩ</td>
</tr>
<tr>
<td>Dielectric withstand</td>
<td>1600 Vrms, between adjacent terminals and terminals to shell, per UL #498</td>
</tr>
</tbody>
</table>

Table 19: Environmental Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature rating</td>
<td>-20 °C to 60 °C</td>
</tr>
<tr>
<td>Protection</td>
<td>IP67, NEMA 6P</td>
</tr>
</tbody>
</table>

Table 20 lists the recommended connectors for a variety of devices and cable types. It is not necessary to use one of these connectors to meet the SERIPLEX standards. However, using the standard connectors reduces problems with network interoperability.

Table 20: Recommended Connectors

<table>
<thead>
<tr>
<th>Receptacle Plug</th>
<th>Receptacle Plug</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-pin micro 5-pin micro</td>
<td>5-pin mini 5-pin mini</td>
</tr>
<tr>
<td>5-pin mini 7-pin mini</td>
<td>7-pin mini 7-pin mini</td>
</tr>
<tr>
<td>Phoenix contact SMSTB or 7006146 45° IDC</td>
<td>Phoenix contact MSTBVA IDC header strip</td>
</tr>
<tr>
<td>AMP 641229-5 IDC AMP 641208-5 IDC</td>
<td>AMP 747840-4 DB9-P</td>
</tr>
<tr>
<td>AMP 747905-4 DB9-S</td>
<td></td>
</tr>
</tbody>
</table>

Note the following requirements for using a micro-style connector:

- Cable assemblies must have Munsell 2.5 YR 6/14 orange cable jackets
- Where possible, the housing and insert must be orange in color to quickly identify SERIPLEX ports
When using a five-pin, mini-style connector with SERIPLEX quick connectors and tee-junction connectors, the pinout described in Figures 22 and 23 and Table 22 is required.

![Figure 22: Five-Pin, Mini-Style Receptacle](image)

![Figure 23: Five-Pin, Mini-Style Plug](image)

**Table 22: Five-Pin, Mini-Style Connector Pin Assignments**

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Function</th>
<th>Description of Connected Wire</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>shield/drain</td>
<td>bare, gray, or orange</td>
</tr>
<tr>
<td>2</td>
<td>V+ bus power</td>
<td>red</td>
</tr>
<tr>
<td>3 (extended)</td>
<td>bus common</td>
<td>black</td>
</tr>
<tr>
<td>4</td>
<td>clock</td>
<td>blue</td>
</tr>
<tr>
<td>5</td>
<td>data</td>
<td>white</td>
</tr>
</tbody>
</table>

When using a seven-pin, mini-style connector with SERIPLEX quick connectors and tee-junction connectors, the pinout described in Figures 24 and 25 and Table 23 is required.

![Figure 24: Seven-Pin, Mini-Style Receptacle](image)

![Figure 25: Seven-Pin, Mini-Style Plug](image)
Table 23: Seven-Pin, Mini-Style Connector Pin Assignments

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Function</th>
<th>Description of Connected Wire</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>shield/drain</td>
<td>bare, gray, or orange</td>
</tr>
<tr>
<td>2</td>
<td>bus power</td>
<td>red</td>
</tr>
<tr>
<td>3</td>
<td>V+ auxiliary power</td>
<td>red with white stripe</td>
</tr>
<tr>
<td>4</td>
<td>V- auxiliary power</td>
<td>black with white stripe</td>
</tr>
<tr>
<td>5</td>
<td>data</td>
<td>white</td>
</tr>
<tr>
<td>6</td>
<td>clock</td>
<td>blue</td>
</tr>
<tr>
<td>7 (extended)</td>
<td>bus common</td>
<td>black</td>
</tr>
</tbody>
</table>

Figure 26: Phoenix Contact Receptacle

Figure 27: Phoenix Contact Header Plug

Figure 28: AMP 641229-5 IDC Receptacle

Figure 29: AMP 641208-5 IDC Plug

Figure 30: DB9-S Receptacle

Figure 31: DB9-P Plug
The following items must be included in product documentation created for users of SERIPLEX products.

- All physical and environmental information necessary to allow a user to properly design a SERIPLEX control system, including:
  - current draw from the bus power line, both during normal operation and device programming
  - bus power voltage range
  - bus data line capacitance
  - bus clock operating range (for example, 10 kHz to 192 kHz)
  - environmental specifications such as temperature, humidity, etc.
  - electrical isolation rating between the SERIPLEX bus and the external I/O points (if applicable)
- A description of the means for connecting the device to the SERIPLEX control bus cable, as well as to the programming device (set-up tool)
- Requirements for the entry of device configuration data, including:
  - how to assign SERIPLEX addresses to the device signals
  - how to enable address multiplexing (if applicable) and assign multiplex channels to device signals
  - how to configure internal logic functions and programmable features such as input and output signal polarity control (if applicable)
  - how to enable and configure optional data error detection mechanisms such as CDR, digital debounce, and data echo
  - conventions for SERIPLEX bus address assignment (for example, addressing multi-bit signals on 16-bit address boundaries)
  - recommended default values for the configuration data in the SERIPLEX ASIC2B network interface chip (including the required input voltage threshold—corresponding to the requirements of the device’s circuit design—to be programmed by the user, if applicable)
  - how to designate a health bit (if available)
- A description of how the device responds to power-up, power-down, and bus fault conditions
- An instruction that users should not defeat the power isolation designed into SERIPLEX devices, since doing so could lessen the integrity of the device and the application, making the system susceptible to electrical transients

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Function</th>
<th>Description of Connected Wire</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>shield/drain</td>
<td>bare, gray, or orange</td>
</tr>
<tr>
<td>2</td>
<td>bus common</td>
<td>black</td>
</tr>
<tr>
<td>3</td>
<td>V+ bus power</td>
<td>red</td>
</tr>
<tr>
<td>4</td>
<td>clock</td>
<td>blue</td>
</tr>
<tr>
<td>5</td>
<td>data</td>
<td>white</td>
</tr>
</tbody>
</table>

10. USER DOCUMENTATION
• Appropriate user safety notifications
  — At a minimum, the SERIPLEX Technology Organization recommends a warning similar to the following:

  It is possible that corrupted information in the control system described in this document can cause the system to report an incorrect input, or incorrectly operate an output. Where personnel and/or equipment hazards exist, use appropriate interlocking. Those responsible for the application, implementation, and use of the control system must ensure that the necessary design considerations have been incorporated into each application, completely adhering to applicable laws, performance and safety requirements, regulations, codes, and standards.

  This system offers significant advantages in communication throughput, I/O number, and control bus length. Proper application will result in a reliable, high-performance control system.

  — The SERIPLEX Technology Organization also recommends inserting a warning that visually attracts attention to the possible need for safety interlocks, such as the following:

  ![WARNING]

  **HAZARD OF UNEXPECTED OUTPUT ACTUATION**

  Where personnel and/or equipment hazards exist, use the appropriate hard-wired safety interlocks.

  Failure to follow this instruction can result in death or serious injury.
11. GLOSSARY

This section defines terms used within this document and within other documents that describe the operation of the SERIPLEX control bus and related devices.

A

address: An integer between 0 and 255 inclusive, that identifies a single bit of SERIPLEX bus input or output data. An address corresponds to a single clock pulse in peer-to-peer operating mode, and corresponds to two consecutive clock pulses in master/slave mode.

address multiplexing: A means of extending the data capacity of a SERIPLEX bus by assigning signals to one of 16 multiplex channels at the same address, and broadcasting the multiplex channel number at the start of each data frame. Each data frame corresponds to a single multiplex channel, and multiplexed devices only respond to the bus during data frames that correspond to their assigned multiplex channels.

address period: The portion of a SERIPLEX bus data frame that corresponds to a specific address. In peer-to-peer operating mode, each address period is one clock period in duration; and in master/slave mode, each address period equals two clock periods.

address sharing: The practice of assigning 2 or more signals to the same address. In the peer-to-peer mode, all addresses used are typically shared by one input signal and one output signal.

analog device: See analog input device and analog output device.

analog input device: A device that converts an external analog signal to a numeric signal to be transmitted to the SERIPLEX bus as bus input data.

analog output device: A device that converts a SERIPLEX bus numeric output signal to an external analog signal.

analog signal: An electrical signal whose value corresponds to either the amount of potential (voltage) measured between 2 points, or the amount of current flowing through a circuit. In general, an analog signal can assume many different values between 2 end limits. The term analog signal is also frequently used to refer to a SERIPLEX bus numeric signal that corresponds to the value of an external analog signal. See also discrete signal, numeric signal.

ASIC: Application-Specific Integrated Circuit; the integrated circuit (IC) or chip that is embedded into SERIPLEX bus I/O devices, enabling them to exchange data signals through a SERIPLEX bus, and to monitor the bus for fault conditions.

ASIC1: The first-generation SERIPLEX bus ASIC, introduced in 1990.

ASIC2B: The second-generation SERIPLEX bus ASIC, introduced in 1996. To the features of ASIC1, it adds improved performance, speed, and flexibility.

B

BFD: See bus fault detection.

binary signal: See discrete signal.

bit: A single unit of binary information; either a 1 or a 0. Short for binary digit.
bleedover: See excess capacitance.

branch: (Network) drop.

bus: A SERIPLEX control bus; the physical connection among SERIPLEX bus devices. This term includes the bus cable, all connected bus devices, and the communications protocol through which bus data is exchanged among devices.

bus cable: The collection of wires that electrically connects SERIPLEX bus devices together, through which the bus data is transmitted. The bus cable typically consists of four individually-insulated conductors surrounded by a foil shield, and housed within a single overall insulating jacket. The four cable conductors correspond to the bus power, common, clock, and data lines.

bus fault detection (BFD) pulse: A negative-going (logic high-to-low-to-high) pulse on the bus data line during the sync period, produced by the bus clock source, and used by the clock source and I/O devices to evaluate the condition of the SERIPLEX bus.

bus halt: A condition in which the SERIPLEX bus clock signal is not operating, so that no data signals are transmitted through the SERIPLEX bus, and all bus output devices assume their default states. A bus halt is essentially the same as a clock loss condition; bus halt is usually used to indicate that the condition is normal and intentionally induced by the clock source.

bus power: The DC voltage applied to the bus communication circuitry of SERIPLEX bus devices through the SERIPLEX bus cable. Typically the source voltage is 24 Vdc, and this power source is electrically isolated from any power sources used to activate control devices or sensors.

byte: A group of 8 bits of SERIPLEX bus input or output data assigned to consecutive signal addresses.

cable propagation delay: The maximum time required for a signal to propagate between any two nodes on the network.

CDR: See complementary data retransmission.

channel: See multiplex channel, input point, output point, signal address, or word.

chip: The SERIPLEX bus application-specific integrated circuit (ASIC).

clock: The SERIPLEX bus signal that is used to synchronize data exchange among bus devices. This is one of the four required conductors within the SERIPLEX bus cable.

clock loss: A condition in which the SERIPLEX bus clock signal is not operating, so that no data signals are transmitted through the SERIPLEX bus, and all bus output devices assume their default states. Clock loss is essentially the same as a bus halt condition; clock loss is usually used to indicate that the clock signal has been halted due to a fault condition, rather than through normal and intentional operation of the clock source.

clock loss detection period: The amount of elapsed time required without a transition of the SERIPLEX bus clock signal (low to high or high to low) for a given bus device to detect a clock loss condition, as opposed to a sync period. For the SERIPLEX ASIC2B chip, this period is nominally 1.5 ms.
Typically, bus output devices will assume their default states once the clock loss detection period has elapsed.

**clock module**: A dedicated device that performs clock source functions for a SERIPLEX bus operating in peer-to-peer mode. Its use generally implies that I/O devices talk directly to each other without the supervision of a host controller.

**clock period**: The elapsed time between two positive (logic low-to-high) transitions of the SERIPLEX bus clock signal during the data-transfer portion of a data frame. This period is the inverse of the clock rate.

**clock pulse**: A sequence of logic level transitions on the SERIPLEX bus clock line, beginning with a positive (logic low-to-high) transition, through a negative (high-to-low) transition, and concluding at the start of the next positive transition. Each clock pulse is one clock period in duration.

**clock rate**: The frequency of the SERIPLEX bus clock signal during the data-transmission portion of a data frame, usually expressed in kHz. This rate is the inverse of the clock period.

**clock source**: A SERIPLEX bus device that generates the bus clock signal, provides the current source for the bus data line, and transmits the bus fault detection pulse. In master/slave mode, the clock source is usually incorporated within an interface to a host controller, but for peer-to-peer mode operation this can be a clock module instead.

**common**: The SERIPLEX bus cable conductor that carries the return current from the bus power supply, and provides a signal reference for the bus clock and data signals. This is one of the four required conductors within the bus cable.

**complementary data retransmission (CDR)**: A method of verifying that the received value of a multi-bit signal matches the value transmitted by the signal source. To accomplish this, the source device sends an encoded version of the signal data with the original signal data, and the receiving device compares the two values.

**control power**: A power source that supplies power for control and sensing devices. Typically this power source is electrically isolated from bus power, both to isolate the SERIPLEX bus from electrical noise sources and so that faults within control and sensing devices do not deprive the SERIPLEX bus system of bus power.

**control software**: Software that monitors SERIPLEX bus input signals and controls bus output signals. This software might be C or Basic code within a computer, ladder logic within a PLC, or embedded firmware within a dedicated control device. Typically this software performs bus start/stop functions and interface card initialization as well as signal monitoring and control.

**daisy chain**: A method of connecting SERIPLEX bus devices by cable segments connected end-to-end. Each segment of bus cable connects to exactly two bus devices, and each bus device connects to exactly two cable segments, except for the two devices at either end of the bus cable. In this cabling method there are no cable loops and no T junctions.

**data**: A SERIPLEX bus signal used to indicate the logic values of bus data signals. This is one of the four required conductors within the bus cable.
data echo: A feature of the SERIPLEX bus ASIC2B in which the ASIC retransmits a discrete bus output signal that it receives back onto the bus as a bus input signal. This feature can be used to indicate to a bus data-transmission device that a data signal has been properly received by another bus device.

data frame: A sequence of clock pulses on the SERIPLEX bus clock line, bounded at its beginning and end by a sync period. Each data frame is used to transmit from 15 to 255 bus input and output signal bits among bus devices.

data line capacitance: Within a bus device, the capacitance measured between the bus data line and the bus common line, at the device’s bus connector. Within a bus cable, the capacitance measured between the bus data line and all other conductors combined.

data pass-through: An interface card feature used in bus master/slave mode, which takes SERIPLEX bus input signals and retransmits them as bus output signals at the same signal addresses, without the intervention of control software. This feature mimics peer-to-peer mode operation in that input devices directly control output devices at the same address without host control programming.

debounce: See digital debounce.

default state: The state assumed by the output signals of the SERIPLEX bus I/O device under a clock loss or bus fault condition. Usually this is the off or inactive state of the output, and corresponds to a bus output signal value of 0. The default state becomes effective after the SERIPLEX bus halts normal operation, and may or may not correspond to the shelf state, which is assumed before the bus begins operating.

device: Any control or sensing device that is electrically connected to the SERIPLEX bus, including both clock sources and I/O devices. The term "device" refers collectively to the bus communications circuitry, to any other circuitry within the device, to any mechanical and/or electromechanical actuators that interface with the device circuitry, and to the device’s physical housing and electrical connectors.

digital debounce: A feature of the SERIPLEX bus devices, in which multiple identical values of a particular discrete bus signal must be detected in successive data frames in order to cause the signal-receiving device to change the logic state of its internal, received signal.

discrete signal: A data signal consisting of exactly one bit of information. Such a signal can assume one of only two states or values—logic high or low, 0 or 1. Both SERIPLEX bus input and output data signals and a device’s external input and output signals can be discrete signals.

driver: See software driver.

drop: A relatively short length of SERIPLEX bus cable that is connected to a longer trunk cable, which in turn is connected to other branches and/or nodes. Typically drop lines are 30 feet or less, while trunk lines can be hundreds or thousands of feet long.

excess capacitance: An effect that occurs when the bus data line cannot recharge to a logic-high state within one-half clock period after being released from a logic-low state. This condition may result in signals with an intended value of 0 being incorrectly interpreted as having a value of 1.
F

frame: See data frame.
frame length: The number of signal addresses transmitted within a single SERIPLEX bus data frame.
frame period: The elapsed time between the end of successive sync periods while a SERIPLEX bus system is operating normally.
frame size: See frame length.
frame time: See frame period.

H

health bit: A discrete SERIPLEX bus input signal that is assigned a fixed value of 1. When the health bit has a value of 0, the system is alerted that there is a problem with the device (such as loss of power or a malfunction) or its connection (such as an open bus cable or connector).
host: See host controller.
host controller: A device that monitors SERIPLEX bus input signals and/or controls bus output signals. Typically the host controller consists of a combination of hardware and software, incorporates the bus clock source, and operates in the master/slave mode, having exclusive access to all bus input data and exclusive control over all bus output signals.
host interface: An electronic hardware device that allows control software running on a host controller to monitor and control I/O devices through a SERIPLEX control bus by some means such as a backplane interface or network gateway. A host interface typically also provides SERIPLEX bus clock source functions.
hysteresis: A voltage barrier that must be overcome in order to induce a change in logic state. For instance, if resting at a logic-low state, the SERIPLEX bus data line must exceed 7.5 Vdc to be recognized as logic high, and if resting at logic high, the data line must drop below 3.0 Vdc to be recognized as logic low; this corresponds to 4.5 V hysteresis.

I

input: See input point or input signal.
input point: An electrical connection to a device, which accepts a single discrete or analog input signal. Usually this term refers to a general-purpose external physical connection to an I/O module.
input propagation delay: The elapsed time between an external input signal event and that signal’s availability within a SERIPLEX bus input device for transmission to the bus.
input response time: In peer-to-peer mode, the elapsed time between an external input signal event and that signal’s appearance on the SERIPLEX bus. In master/slave mode, the elapsed time between an external input signal event and that signal’s availability to a host controller’s internal logic processor.
**input signal**: A signal sensed by a SERIPLEX bus device other than a host controller, and reported to the SERIPLEX bus.

**interface, interface card**: See host interface.

I/O (input/output): Devices that sense input signals and/or drive output signals that are external to the SERIPLEX bus.

**I/O module**: A device that translates between SERIPLEX bus signals and external physical signals. An I/O module generally refers to devices supporting general-purpose input and output points that can connect to a variety of control and/or sensing devices, as opposed to a dedicated device that incorporates a control or sensing function as well as bus communication. Typically, I/O modules use a SERIPLEX bus ASIC to perform bus communication functions. Most I/O modules use an optical isolation barrier between the bus and external input and output points.

**I/O point**: See input point, output point.

**isolation**: A galvanic separation between two or more electrical circuits, so that no direct current flows between the circuits, and there is no direct relationship between the potential of the circuits as compared to a common reference point. Most SERIPLEX bus devices provide isolation between the bus and any other logic or I/O circuitry within the device, both to improve noise immunity and to prevent external fault conditions from affecting the operation of the SERIPLEX bus.

**junction**: A passive electrical connection among segments of SERIPLEX bus cable. A junction is not a node, in that it contains no electronic bus-interface circuitry.

**logic high**: A discrete signal state in which the DC voltage level of the signal exceeds a designated threshold value. In the case of SERIPLEX bus clock and data signals the logic-high threshold is nominally +7.5 Vdc; for the data line this corresponds to a signal value of 0.

**logic low**: A discrete signal state in which the DC voltage level of the signal is below a designated threshold value. In the case of SERIPLEX bus clock and data signals the logic-low threshold is nominally +3.0 Vdc; for the data line this corresponds to a signal value of 1.

**long reset**: See bus halt, clock loss.

**long reset period**: See clock loss detection period.

**loop**: A SERIPLEX bus cable configuration with a circular data path; a path can be traced along cable segments back to a given starting point without reversing direction along any segment. A loop configuration provides some inherent redundancy in that continuity is maintained to all bus devices in the event of a single cable break.
master: A SERIPLEX bus device capable of monitoring bus input data and transmitting bus output data, especially in the bus master/slave mode. Typically a bus master executes control logic, incorporates the clock source function, has exclusive access to bus input data, and is the only device that transmits bus output data.

master/slave mode: A SERIPLEX bus operating mode intended to enable a bus master device to have exclusive access to all bus input data and exclusive control of all bus output data. In this mode, two bus clock pulses are transmitted per address—one for input data and the other for output data. Also known as Mode 2.

mode 1: See peer-to-peer mode.

mode 2: See master/slave mode.

module: See I/O module.

multi-bit signal: A SERIPLEX bus signal that consists of a grouping of consecutive discrete bus input or output signals. The signal data can represent a numeric value, a set of discrete I/O signals, or some other form of complex data such as ASCII characters.

multiplexing: See address multiplexing.

multiplex channel: An integer between 0 and 15 that serves as an extension of the signal address of devices that support address multiplexing.

node: An electrical connection to the SERIPLEX bus. Typically nodes consist of a clock source or I/O devices including I/O modules and dedicated devices. Passive connections such as T-junctions are not nodes.

noise: Any external signal (a signal other than bus signals) induced into the SERIPLEX bus cable.

numeric signal: A group of consecutive SERIPLEX bus input or output data bits that together represent a single binary number. Numeric signals are frequently used to carry analog signal data. The allowable range of a numeric signal value is determined by the number of bits assigned to that signal (typically 8, 12, or 16). Such signals are usually assigned a starting signal address that is a multiple of 16 (16, 32, ..., 240). See also analog signal.

output: See output point or output signal.

output point: An electrical connection to a device, which drives a single discrete or analog output signal. Usually this term refers to a general-purpose external physical connection to an I/O module.

output propagation delay: The elapsed time between a change in the logic state of an output signal within a SERIPLEX bus device and the corresponding change in state of its external output signal.
output response time: In peer-to-peer mode, the elapsed time between a signal's appearance on the SERIPLEX bus and the corresponding change in state of an external output signal. In master/slave mode, the elapsed time between a signal's assertion by the host controller's internal logic processor (usually into an interface card's memory) and the corresponding change in state of an external output signal.

output signal: A signal received through the SERIPLEX bus by a device other than a host controller, and used to control an external device or signal.

pass-through: See data pass-through.

peer-to-peer mode: A SERIPLEX bus operating mode in which input devices control output signals directly without the intervention of a host controller. In this mode, one clock pulse is transmitted per address, and bus input and output data are sampled at the same time.

point: See input point, output point.

power: The SERIPLEX bus conductor that supplies energy to the bus-interface circuitry of all SERIPLEX bus devices, including the clock source and I/O devices. This is one of the four required conductors within the bus cable.

power supply: A device that supplies a DC voltage source for either the SERIPLEX bus or for external I/O signals. Each SERIPLEX bus system requires at least one bus power supply, and most systems will also use at least one control power supply.

propagation delay: See input propagation delay, output propagation delay.

recommended practice: A device or system design feature not strictly required to ensure interoperability of SERIPLEX bus devices, but that is recommended for reasons of consistency, design margin, or good engineering practice.

SERIPLEX set-up tool: A device for entering addresses and other configuration data into SERIPLEX bus I/O devices using a SERIPLEX bus ASIC. The set-up tool can also be used to read set-up data from I/O devices.

shelf state: The state assumed by the output signals of the SERIPLEX bus I/O device under power loss conditions, and retained until bus operation is initiated. Usually, this is the off or inactive state of the output, and corresponds to a bus output signal value of 0. The shelf state is assumed before the SERIPLEX bus begins operating, and may or may not correspond to the default state of the output, which becomes effective after the bus has halted normal operation.

shield: A braided or foil conductive wrapping around the signal wires in the SERIPLEX bus cable, intended to minimize the amount of noise induced into bus signal conductors. In most installations, it should be connected to the bus common line and to earth ground at exactly one point.
signal: A unit of information transmitted between control and/or sensing devices. A signal can be embodied as a discrete or analog electrical voltage or current, or as a bit or group of data bits transmitted through a SERIPLEX bus.

signal address: For a discrete signal, the bus address corresponding to the signal's data. For a multi-bit signal, the address corresponding to the first (least significant) bit of the signal's data.

signal reflection: A secondary signal that is induced on either the bus clock or data line when the primary signal reaches a discontinuity in cable impedance, such as a cable branch or the end of the bus cable. Depending upon the cable configuration and system settings, these reflections either amplify or attenuate the primary signal. Most signal reflections are ignored by SERIPLEX bus devices due to their high hysteresis thresholds, so that termination resistors are usually not required.

signal update time: The elapsed time between successive transmissions of a particular signal through the SERIPLEX bus. For non-multiplexed signals, the signal update time equals the frame period. For multiplexed signals, the signal update time usually equals the frame period multiplied by the number of multiplex channels scanned by the clock source.

slave: In master/slave mode, any SERIPLEX bus device that does not generate the bus clock signal.

software driver: A software program or routine providing an interface between control software and an interface card. Typically a driver is used to isolate the control software from the interface card hardware, so that little knowledge of interface card operation is needed by the control software programmer.

star: A SERIPLEX bus cable configuration having multiple branches originating from a single node.

sync period: A pause in the SERIPLEX bus clock signal at the end of each data frame, causing all bus I/O devices to reset their address counters, and therefore synchronizing data transmission among bus devices. A sync period is at least 8 clock periods long and less than the clock loss detection time.

system: A collection of devices that serve to exchange data signals through a SERIPLEX bus control bus in order to perform a given task. At a minimum, a SERIPLEX bus system would consist of a clock source, some I/O devices, bus cable, and a bus power supply; other potential system elements might include a host controller, control software, and a control power supply.

system capacitance: See data line capacitance.

system response time: The elapsed time between an external input signal event and a resulting change in state of an external output signal. System response time factors include input response time, output response time, host controller processing time, and I/O device propagation delays.

throughput: The rate at which actual bus data signals are transmitted through the SERIPLEX bus, usually expressed as kbits/s. This rate is a function of bus address usage (used vs. unused signal addresses) as well as frame length and clock rate.

throughput time: See input response time, output response time, or system response time.
tree: Any SERIPLEX bus cable configuration that includes branches (drops).

trunk: A relatively long section of SERIPLEX bus cable from which one or more drops originate.

trunk-and-drop: A SERIPLEX bus cable configuration consisting of a single long cable with several short branches distributed along its length.

wire-AND: A logic function resulting from assigning multiple discrete output devices to the same SERIPLEX bus address, where activating the corresponding bus output signal causes all of these devices to turn on.

wire-OR: A logic function resulting from assigning multiple discrete input devices to the same SERIPLEX bus address, where activating any of these input devices results in the assertion of the corresponding bus input signal.

word: A group of 16 bits of SERIPLEX bus input or output data assigned to consecutive signal addresses, with the starting address being an integer multiple of 16 (0, 16, 32, ..., 240).
Appendix A—Messaging Protocol

INTRODUCTION

The SERIPLEX control bus is designed to exchange control signals quickly and deterministically among control and sensing devices. However, many applications also require the exchange of parameters, files, and other information not directly involved in real-time control. Compared to a typical SERIPLEX control signal transmission, such general-purpose data transmission typically contains much more data, but does not require transmission as quickly or deterministically.

This appendix defines a messaging protocol for the performance of general-purpose data transmission, as described above. The protocol uses a defined portion of the SERIPLEX bus data, while leaving most of the bus available for more typical control signal transmissions. In this way, intelligent devices can exchange general-purpose data through a SERIPLEX bus without interfering with real-time control performed through the same bus.

The requirements of the SERIPLEX network messaging protocol are as follows:

1. Provides support for network messaging concurrently with the existing SERIPLEX protocol
2. Does not invalidate existing devices
3. Supports transmission of messages (theoretically) of any length
4. Includes an addressing scheme that supports the end-to-end communication of message transactions in a client/server fashion
5. Supports the broadcasting of messages
6. Includes a bus access and arbitration scheme that supports prioritization of messaging in a way that guarantees delivery of high priority messages in a timely fashion
7. Includes an object addressing scheme that supports object-to-object communication of service requests and responses

The components of the SERIPLEX network messaging protocol are presented in the following sections. They include:

1. Data transmission: the mechanism for transmitting message data in SERIPLEX networks
2. Network access and addressing: the method by which SERIPLEX nodes gain access to the network for transmitting messages
3. Message structure: the fields/protocol within a SERIPLEX message
4. Object addressing protocol: the protocol within the message structure utilized for object-to-object communication of service requests and responses

This document also describes the mechanism by which message-capable nodes can coexist with message-incapable nodes in a SERIPLEX network.

GLOSSARY

Operating cycle — A period of time during which a SERIPLEX network device is capable of supporting the communication (transmission and/or reception) of SERIPLEX-formatted information. Note that an interruption in power or a halt of the SERIPLEX bus will end an operating cycle. Note also that an operating cycle of a device will end if that device senses that it is no longer capable of sending or receiving SERIPLEX information, e.g., if the device is disconnected from the network or reset by a user.
Messaging is supported in both peer-to-peer and master/slave configured networks, as well as in both multiplexed and non-multiplexed communication schemes. In all cases messages are communicated serially in the last 16-bit word of each channel, as shown in Figure 32a. This word is called the message field. Output bits 12 through 15 in the reserved (non-multiplexed) area of each channel form the frame length field and indicate the 16-bit boundary where the message field begins in each channel. This relationship is summarized in Table 1. The data for the frame length field must be generated by the network host or by another designated device. Note that a value of 0000 for the frame length field indicates that messaging is not supported.

All SERIPLEX nodes that support and wish to utilize messaging should monitor the frame length field to determine the location of the message field on each channel. A device must redetermine the frame length at the start of any new operating cycle (i.e., after a bus halt or a power cycle). The four bits of the frame length field should remain constant throughout the operating cycle of a network. A device determines that the four bits are constant by going through a debounce procedure three times (i.e., reading the field three times in successive frames for consistency). If the bits remain constant through this debounce procedure, the device should ignore any subsequent changes to any of these four bits during the current operating cycle and can thus effectively ignore the field. Note that a device cannot begin to send or receive messages using the messaging protocol until it has successfully completed this debounce procedure.

The data that is transmitted serially in the message field comprises SERIPLEX messages. These messages are transmitted in one or more sequential fragments that together comprise the message. The components (also called fields) of a SERIPLEX message fragment are shown in Figure 32b. These components and the SERIPLEX message fragmentation scheme are explained in the following sections.
Messaging is supported in a publish/subscribe fashion in the SERIPLEX protocol whereby all nodes may monitor any message transmitted. An addressing scheme is utilized within this messaging protocol to provide client/server-type point-to-point communication within this publish/subscribe protocol.

Specifically, the SERIPLEX messaging protocol requires that all nodes wishing to utilize messaging have a configurable, unique messaging address in the SERIPLEX network. Valid messaging addresses range between 1 and 255. It is the responsibility of the person configuring the network to set up node messaging addresses as necessary to guarantee uniqueness.

When a node wishes to send a message, it monitors a messaging busy field in the SERIPLEX frame (see Figure 1) to see if the message field is currently being utilized by another node to send a message. The messaging busy field, which is input bit 10 in the reserved (non-multiplexed) portion of the data frame, has a value of 1 when the message field is busy and a value of 0 when it is idle. If a node wishing to send a message determines that the messaging busy field is set to 0 (idle), it sets the messaging busy field to 1 (busy) in the next frame and begins sending its message in the message field of that next data frame.

The SERIPLEX messaging protocol utilizes message and node prioritization along with bitwise arbitration to determine unique node access to messaging. This protocol is thus utilized to resolve conflicts in situations where multiple nodes wish to begin transmitting messages in the same frame. As shown in Figure 2, the first 16 bits of each message, called the arbitration field, contains a message priority and a source (i.e., sending) messaging address. Note that because it contains the unique source

---

1. Address zero is reserved for broadcasting, which will be described later.
2. Future versions of the messaging protocol are planned to support duplicate address detection.
3. Note that this arbitration scheme applies to all nodes except the host in a master/slave configured network. This is discussed further in the next section.
messaging address of the sending node, no two messages originating from different nodes can have the same arbitration field value.

This uniqueness quality is used in the messaging protocol for bus arbitration. When a node wishes to transmit a message and sees that the message field is available, it begins to write the arbitration field of its message (containing the sender’s messaging address and message priority) into the message field, bit by bit. If more than one node wishes to send a message, then multiple nodes begin writing to the message field. As each bit address in the message field is written to the bus by a node, it immediately reads back the value at that address to see if it is the same as the value written. If the value written is different than the value read, the node immediately stops transmitting its message. If a node is able to write and read back its entire arbitration field, that node has won access to the message field and may send its message fragment. It then keeps the messaging busy field set to 1 (busy) and sends its message fragment (see “Message Structure” on page 67). It sets the messaging busy field back to 0 (idle) in the frame that will contain the last word of the message fragment (in the message field), thus indicating that the message field is available for sending arbitration of the next fragment.

The SERIPLEX protocol physical signaling is configured such that logic 1 dominates over logic 0. Thus for example, if one node asserts a logic 0 to an address in a frame and a second node asserts a logic 1 to that same address, the address will resolve to a logic 1. Because, as noted above, no two messages originating from different nodes can have the same arbitration field value, it is guaranteed that exactly one node among those attempting to send a message will not have any of its arbitration field overwritten.

This arbitration mechanism is illustrated in the example presented in Figure 34. Note that, in this case, both nodes 152 and 204 stop transmitting and node 130 gains exclusive access to the message field.
MESSAGE STRUCTURE

Each SERIPLEX message, transmitted serially in the message field, consists of one or more sequential message fragments. Each message fragment contains seven fields as shown in Figure 32b. Table 26 contains a description of each of these fields. Note that a message contains both a source and destination messaging address for node-to-node routing.

Table 26: Fields in a Message Fragment

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Size (bits)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ar Bryant **</td>
<td>16</td>
<td>Includes 3 bits (set to 0, 1, and 0 respectively) reserved for future use: message priority (5 bits); and sender’s “source” messaging address (8 bits). Used in a bitwise-arbitration fashion by a node to obtain access to the message field in a SERIPLEX data frame.</td>
</tr>
<tr>
<td>Destination Messaging Address</td>
<td>8</td>
<td>Destination node messaging address for the message. A value of 0 indicates a message broadcast (intended for all nodes listening to messages).</td>
</tr>
<tr>
<td>Data Fragment Length</td>
<td>4</td>
<td>The length of the entire fragment (in 16-bit words), including the arbitration word and the destination messaging address word, but not including the CRC word. Its value must be between 3 and 15.</td>
</tr>
<tr>
<td>Fragment Sequence Number</td>
<td>3</td>
<td>A counter indicating the sequential fragment number, beginning with 000, 001, 010, …, 111. The counter rolls over from 111 to 000.</td>
</tr>
<tr>
<td>Last Fragment Indicator</td>
<td>1</td>
<td>A value of 1 (true) Indicates the last fragment in the message.</td>
</tr>
<tr>
<td>Data Fragment: Object Addressing Protocol</td>
<td>Multiples of 16 (from 16–208)</td>
<td>Fragment of message data that contains the object addressing protocol for object-to-object communication. This protocol is described in the next section.</td>
</tr>
<tr>
<td>CRC</td>
<td>16</td>
<td>A frame check sequence derived from a cyclic redundancy code (CRC). The calculation and use of this field is described later in this document.</td>
</tr>
</tbody>
</table>

* All fields are transmitted LSB first.
** The arbitration field is not used in master messaging (see below).

The data (i.e., object addressing protocol) portion of messages is broken into smaller fragments so that high-priority messages can gain access to the network in a timely fashion. A message fragment must be less than or equal to 15 words (not including its one-word CRC field). When a node prepares to send a message longer than the maximum fragment length, it must break up the object addressing protocol field of the message into sequential fragments of 13 words or less each, and construct message fragments (of 15 or fewer words) consisting of the fields described in Table 2. The node must utilize bitwise arbitration as described in the previous section to gain access to the message field for the sending of each fragment. Thus if a node wishes to send a higher priority message while another node is sending a low priority message, it may arbitrate for access to the message field after the current fragment is sent.

Host Messaging Protocol in a Master/Slave Configuration

The network arbitration scheme mentioned in the previous section applies to all message-capable nodes in a peer-to-peer network system, and to all message-capable slaves in a master/slave system. The host in a master/slave network configuration has exclusive control of the output portion of the bus bandwidth. Thus it does not need to utilize the arbitration scheme to gain access to the network. The host sets the source address (in the arbitration field) to 0. In master/slave operation only, output address 9 is assigned to a host send (one-bit) field. When this field is set to 1, it means that the host is sending the first word of a message. Messaging-capable slaves should look to this first message word, which contains the destination messaging address field (see Table 26 and Figure 32b), to see if the message is meant for them. The host can indicate a broadcast message by setting the destination messaging address field to 0.
OBJECT ADDRESSING PROTOCOL

The data fragment portions of the message fragments, when concatenated at a node, form the data field portion of the message. This data is formatted according to the object addressing protocol, that is, the protocol used for object-to-object communication between nodes.

The objects, their groupings, structure, and behavior in SERIPLEX devices conform to an object model. In this model, objects are generally regarded as entities that group structure and behavior in a logical manner. Objects usually have a physical or conceptual analog in a device application. For example, an object may be associated with a sensor in a device, or may be the collection of structure and behavior that comprises the management of the device. The SERIPLEX object addressing protocol utilizes a class-instance hierarchy to support inheritance to allow for the definition of “types” of objects (classes) as well as specific implementations of these objects (instances). For example, an object class in a photodetector array device might be “photodetector,” while object instances refer individually to each photodetector.

An object (class or instance) has zero or more attributes, which are parameters that contain information associated with the device. For example “sensor value” may be a parameter associated with a sensor object instance.

An object (class or instance) supports zero or more services, which are functions or capabilities that the object can provide. Most services are request services in which a “request” for a service is issued to an object, and the object generates a specific “response” to the requestor as part of the process of carrying out the service request. Parameters may be included with the request and/or response as necessary to carry out the service. As an example, a service supported by a sensor object may be “get” where an associated request parameter is “attribute number” and an associated response parameter is “attribute value.” An object may also support notification services. “Notifications” associated with these services are generated asynchronously by the object. Parameters may be included with the service notification as necessary to carry out the service. As an example, an alarm publish service may be associated with a sensor object and would report an alarm state attribute whenever that attribute changes from zero to a non-zero value.

An object also has associated behavior, which identifies as appropriate how the object implements services, interacts with other objects, interacts with any outside environment, etc. For example, behavior associated with a sensor object might be: on receipt of “get” service request, where attribute number parameter corresponds to “value” attribute, detect environment value, store in “value” attribute, and send “get” service response with response parameter value equal to “value” attribute.

The object addressing protocol utilized in the data field of SERIPLEX messaging provides for the communication of services (requests, responses, and notifications) between objects at various message-capable nodes on the SERIPLEX network, thereby supporting the SERIPLEX object model. In order to provide this support, the data field of a message is sub-divided into a number of sub-fields as shown in Figure 4. These sub-fields are described in Table 3.
A SERIPLEX message communicates a service request, response, or notification to or from a specific object instance of an object class at a node using the object addressing protocol. In this way the structure/behavior of an object can be communicated/invoked over a SERIPLEX network using SERIPLEX messages.
FRAGMENT DATA VERIFICATION:
THE CRC FIELD

The last 16-bit word of each fragment transmitted is the CRC (cyclic redundancy check) field (see Table 26). This field is used to verify the correctness of the fragment data. The value of the field is the remainder result of a fragment polynomial divided (modulo-2) by a generator polynomial. The fragment polynomial coefficients are given by the bit stream, consisting of the entire fragment from the arbitration field up through the end of the data fragment field (i.e., not including this CRC field). The fragment polynomial is arranged so that the fragment LSB (transmitted first) corresponds to the highest-order term of the polynomial. The generator polynomial is:

\[ X^{16} + X^{15} + X^2 + 1 \]

In each fragment to be transmitted, the sender first multiplies the fragment polynomial by \( X^{16} \) then divides the result by the generator polynomial to determine the remainder. This remainder is inserted in the CRC field at the end of the message (highest-order term or LSB first), and transmitted with the fragment. All message-capable nodes to which the fragment is addressed (i.e., nodes with messaging address equal to destination messaging address field value, or all message-capable nodes excluding sender if destination messaging address field is 0) must use the same CRC calculation procedure on the received fragment and determine the remainder value. If the remainder is 0, the fragment is considered verified and may be utilized. If the remainder is non-zero, the receiving node determines that there was an error in transmission and the fragment is discarded. If this fragment is part of a larger message, the receiving node may choose to discard the message entirely including any fragments associated with the message received before or after the erroneous fragment. Alternatively, if the receiving node has the capability to identify the sender of the erroneous fragment, it may choose to parse correctly-received fragments associated with the message. It may then utilize this information to inform the sender (either through a service error response or service error indication) that the message was received in error. The receiving node may not utilize any portion of that message for any other purpose.

COMPATIBILITY OF MESSAGING WITH MESSAGE-INCAPABLE NODES

A large number of SERIPLEX devices do not support a messaging capability for reasons of simplicity, memory conservation, data requirements, etc. These message-incapable devices can co-exist with message-capable devices in a SERIPLEX network. The message-incapable devices do not have to monitor and cannot write to fields in the frame associated with messaging (such as the message field, messaging busy field, etc.). Additionally, these nodes do not have a messaging address, thus a SERIPLEX network can support 255 message-capable nodes. Note that nodes may be set up that cannot transmit messages, but can receive messages. Further, in some network configurations, groups of these receive-only message nodes can be assigned to the same messaging address.